NAND Flash Memory

FBNL05B128G1KDBABJ4-5AF

Features

- Open NAND Flash Interface (ONFI) 4.0 compatible[1]
- JEDEC NAND Flash Interoperability (JESD230B) compatible[2]
- Multiple-level cell (MLC)
- Organization:
  - Page size ×8: 18,592 bytes (16,384 + 2,208 bytes)
  - Block size: MLC: 512 pages, (8192K + 1104K bytes)
  - Plane size: 4 planes × 548 blocks per plane
  - Device size MLC: 128Gb: 2192 blocks
- NV-DDR2 I/O performance:
  - Up to NV-DDR2 time mode 8
  - Clock rate: 3.75ns (NV-DDR2)
  - Read/write throughput per pin: 533MT/s
- NV-DDR I/O performance:
  - Up to NV-DDR time mode 5
  - Clock rate: 10ns (NV-DDR)
  - Read/write throughput per pin: 200MT/s
- Asynchronous I/O performance:
  - Up to synchronous time mode 5
  - ^{t}RC/^{t}WC: 20ns (MIN)
  - Read/write throughput per pin: 50MT/s
- Array performance
  - Snap READ operation time: 42µs (TYP)[3]
  - Single-plane EXPRESS READ PAGE operation time: 57µs (TYP)[3]
  - Multi-plane EXPRESS READ PAGE operation time: 59µs (TYP)[3]
  - Single-plane READ PAGE operation time: 59µs (TYP)[3]
  - Multi-plane READ PAGE operation time: 61µs (TYP)[3]
  - Effective program page: 750µs (TYP)
  - Erase block: 10ms (TYP)
- Command set: ONFI NAND Flash Protocol
- Advanced Command Set:
  - Program Cache
  - Multi-plane commands
  - Multi-LUN operations
  - Copyback
  - Read Retry[5]
- Consult factory for approved controller list
- Operation status byte provides software method for detecting:
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Data strobe (DQS) signals provide a hardware method for synchronizing data DQ in the NV-DDR/NV-DDR2 interface
- Copyback operations supported within the plane from which data is read
- Quality and reliability[5]
  - Testing methodology: JESD47
  - Data retention: See qualification report - May vary for targeted application
  - Endurance MLC/SLC: 1500/15,000 PROGRAM/ERASE cycles
- Operating Voltage Range
  - V_{CC}: 2.7–3.6V
  - V_{CCQ}: 1.7-1.95V
- Operating temperature: 10°C to +70°C
- Package:
  - 132-ball BGA
- RESET (FFh) required as first command after power-on

Notes: 1. The ONFI 4.0 specification is available at http://www.onfi.org/

2. The JEDEC specification is available at: https://www.jedec.org/standards-documents
3. Contact factory for technical details regarding randomization. Array read times listed are without internal randomization.
4. ODT functionality is supported only in NV-DDR2.
5. Read Retry operations are required to achieve specified endurance and for general array data integrity.
6. For the definition of Gib, refer to IEEE 1541-2002 (www.ieee.org)

Part Numbering Information

SpecTek NAND Flash devices are available in several different configurations and densities (see Figure 1).

Figure 1: Marketing Part Number Chart

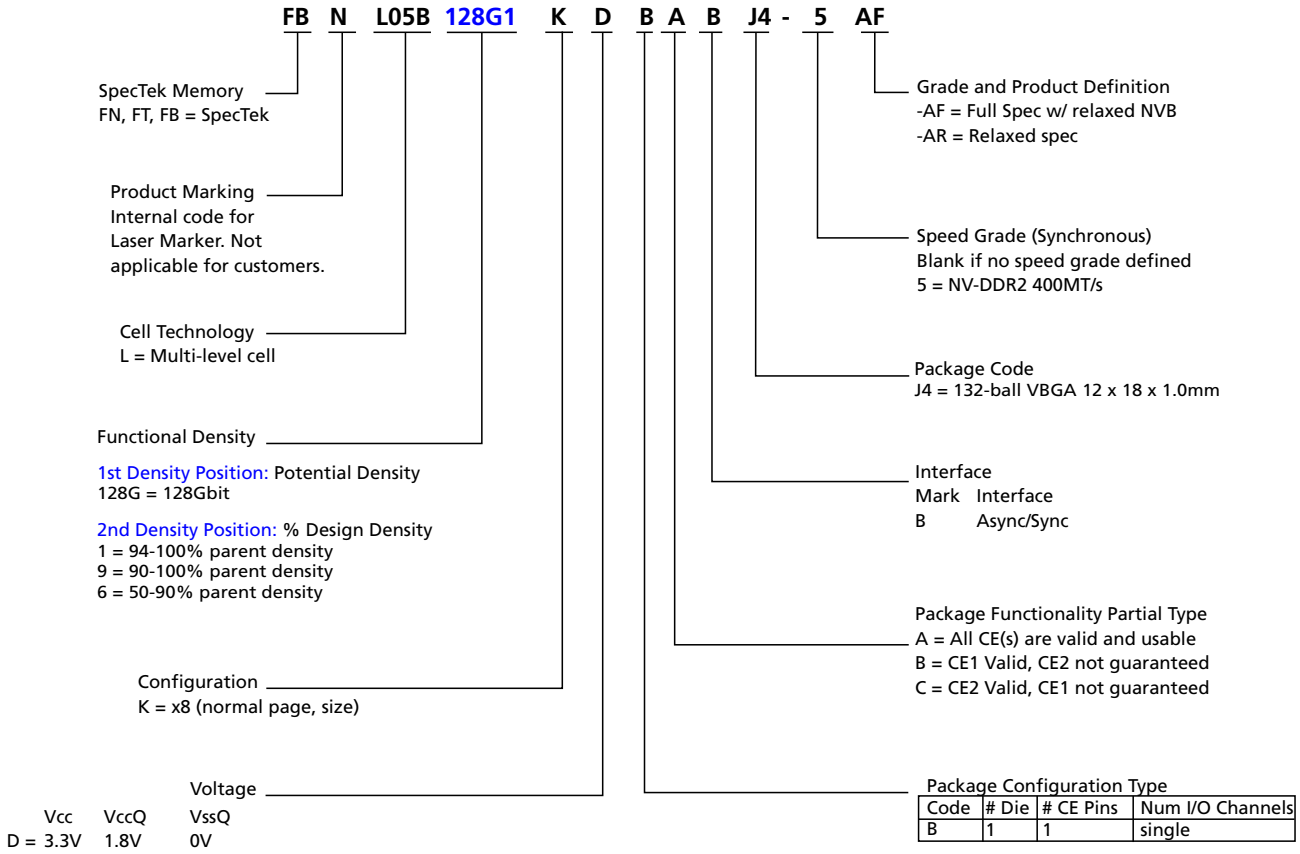

Table 1: Flash Product Type Definitions

Product Type	Name	Description
-AF	Relaxed NVB	Product meets the full specifications with additional screening: READ ID Byte 0 = 0x2C.
-AR	Relaxed Density	Product is allowed to have lower Valid Blocks (N_{VB}) and ICC Standby current (CMOS). See technical note: (Tech Note -- AR Grade).

Valid Part Number Combinations

After building the part number from the part numbering chart, verify that the part is offered and valid by using the SpecTek Parametric Part Search Web Site at: www.spectek.com/menus/distributors.aspx. If the device required is not on this list, contact the factory.

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General Description

SpecTek NAND Flash devices include an asynchronous data interface for I/O operations. These devices use a highly multiplexed 8-bit bus (DQx) to transfer commands, address, and data. There are five control signals used to implement the asynchronous data interface: CE#, CLE, ALE, WE#, and RE#. Additional signals control hardware write protection (WP#) and monitor device status (R/B#).

Some versions of this Micron NAND Flash device additionally includes a NV-DDR and/or a NV-DDR2 data interface for high-performance I/O operations. When the NV-DDR interface is active, WE# becomes CLK and RE# becomes W/R#. Data transfers include a bidirectional data strobe (DQS).

This hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another, enabling future upgrades to higher densities with no board redesign.

A target is the unit of memory accessed by a chip enable signal. A target contains one or more NAND Flash die. A NAND Flash die is the minimum unit that can independently execute commands and report status. A NAND Flash die, in the ONFI specification, is referred to as a logical unit (LUN). For further details, see Device and Array Organization.

These NAND devices are ONFI 4.0 compatible. The ONFI 4.0 specification can be found at www.onfi.org.

Asynchronous, NV-DDR, and NV-DDR2 Signal Definitions

Table 2: Asynchronous, NV-DDR, and NV-DDR2 Signal Definitions

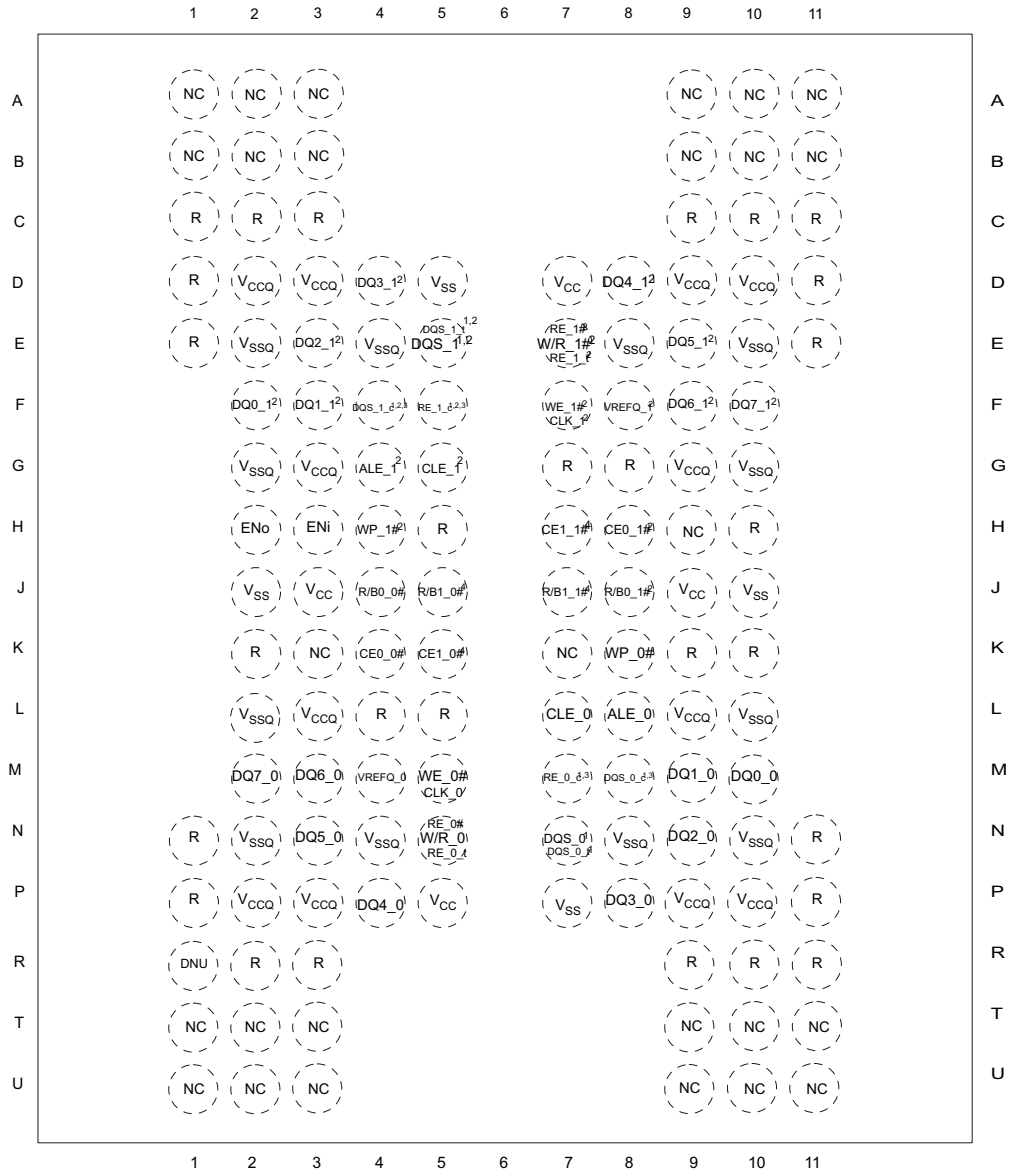
Symbol[1]			Type	Description[2]
Async Signal	NV-DDR Signal	NV-DDR2 Signal		
ALE	ALE	ALE	Input	**Address latch enable:** Loads an address from DQx into the address register.
CE#	CE#	CE#	Input	**Chip enable:** A signal that enables or disables one or more LUNs in a target[1].
CLE	CLE	CLE	Input	**Command latch enable:** Loads a command from DQx into the command register.
DQx	DQx	DQx	I/O	**Data inputs/outputs:** The bidirectional I/Os transfer address, data, and command information.
N/A	DQS	DQS, DQS_t	I/O	**Data strobe:** Provides a synchronous reference for data input and output.
N/A	N/A	DQS_c	I/O	**Data strobe compliment:** Provides a complementary signal to the data strobe signal optionally used in the NV-DDR2 interface for synchronous reference for data input and output.
ENi	ENi	ENi	Input	**Enumerate input:** Input to a NAND device (if first NAND device on the daisy chain have as NC) from ENo of a previous NAND device to support CE# pin reduction functionality.
ENo	ENo	ENo	Output	**Enumerate output:** Output from a NAND device to the ENi of the next NAND device in the daisy chain to support CE# pin reduction functionality.
RE#	W/R#	RE#, RE_t	Input	**Read enable and write/read:** RE# transfers serial data from the NAND Flash to the host system when the asynchronous interface is active. When the synchronous interface is active, W/R# controls the direction of DQx and DQS.
–	–	RE_c	Input	**Read enable complement:** Provides a complementary signal to the read enable signal optionally used in the NV-DDR2 interface for synchronous reference for data output.
WE#	CLK	WE#	Input	**Write enable and clock:** WE# transfers commands, addresses, and serial data from the host system to the NAND Flash when the asynchronous interface is active. When the synchronous interface is active, CLK latches command and address cycles.
WP#	WP#	WP#	Input	**Write protect:** WP# is a signal that enables or disables array PROGRAM and ERASE operations.
R/B#	R/B#	R/B#	Output	**Ready/busy:** An open-drain, active-low output that requires an external pull-up resistor. This signal indicates target array activity.
V_{CC}	V_{CC}	V_{CC}	Supply	**V_{CC}:** Core power supply
V_{CCQ}	V_{CCQ}	V_{CCQ}	Supply	**V_{CCQ}:** I/O power supply
V_{SS}	V_{SS}	V_{SS}	Supply	**V_{SS}:** Core ground connection
V_{SSQ}	V_{SSQ}	V_{SSQ}	Supply	**V_{SSQ}:** I/O ground connection
–	–	V_{REFQ}	Supply	**V_{REFQ}:** Reference voltage used with NV-DDR2 interface.
NC	NC		—	**No connect:** NCs are not internally connected. They can be driven or left unconnected.
DNU	DNU		—	**Do not use:** DNUs must be left unconnected.
RFU	RFU		—	**Reserved for future use:** RFUs must be left unconnected.

Notes: 1. See Device and Array Organization for detailed signal connections.

2. See "Bus Operation – Asynchronous Interface" on page 20, "Bus Operation – NV-DDR Interface" on page 27, and "Bus Operation – NV-DDR2 Interface" on page 34 for detailed asynchronous, NV-DDR, and NV-DDR2 interface signal-use explanations.

Signal Assignments

Figure 2: 132-Ball VBGA (Ball-Down, Top View)



Notes: 1. N/A: This signal is tri-stated when the asynchronous interface is active.
2. These signals are available on dual and quad die packages. They are NC for other configurations.
3. These signals are available when differential signaling is enabled.
4. These signals are available on quad LUN four CE# stacked packages. They are NC for other configurations.

Architecture

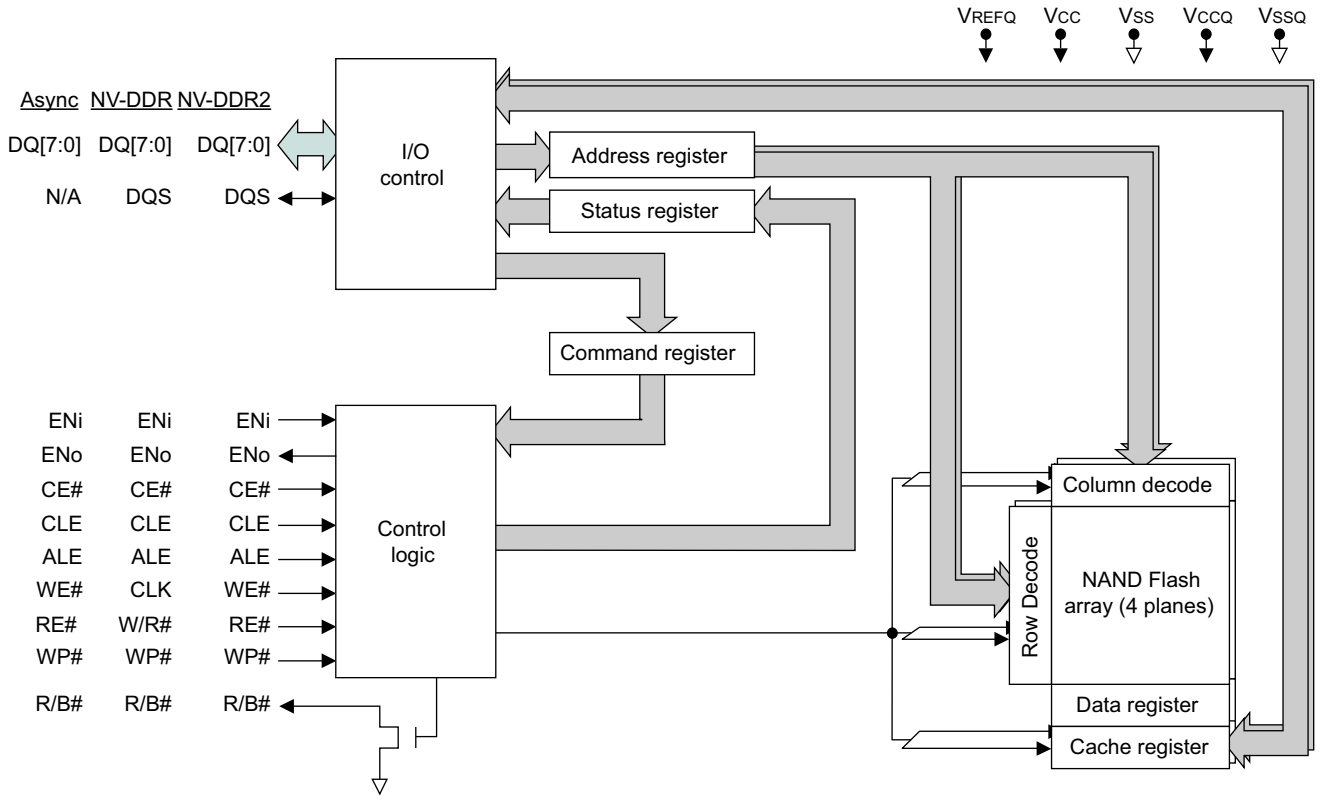
These devices use NAND Flash electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins and received by I/O control circuits. The commands received at the I/O control circuits are latched by a command register and are transferred to control logic circuits for generating internal signals to control device operations. The addresses are latched by an address register and sent to a row decoder to select a row address, or to a column decoder to select a column address.

Data is transferred to or from the NAND Flash memory array, byte by byte, through a data register and a cache register.

The NAND Flash memory array is programmed and read using page-based operations and is erased using block-based operations. During normal page operations, the data and cache registers act as a single register. During cache operations, the data and cache registers operate independently to increase data throughput.

The status register reports the status of die (LUN) operations.

Figure 3: NAND Flash LUN Functional Block Diagram



Notes: 1. N/A: This signal is tri-stated when the asynchronous interface is active.
2. Some devices do not include the NV-DDR or NV-DDR2 interface.
3. Some devices do not include the V_{REFQ} signal.

Device and Array Organization

Figure 4: Device Organization for Single-Die Package, Package Code B

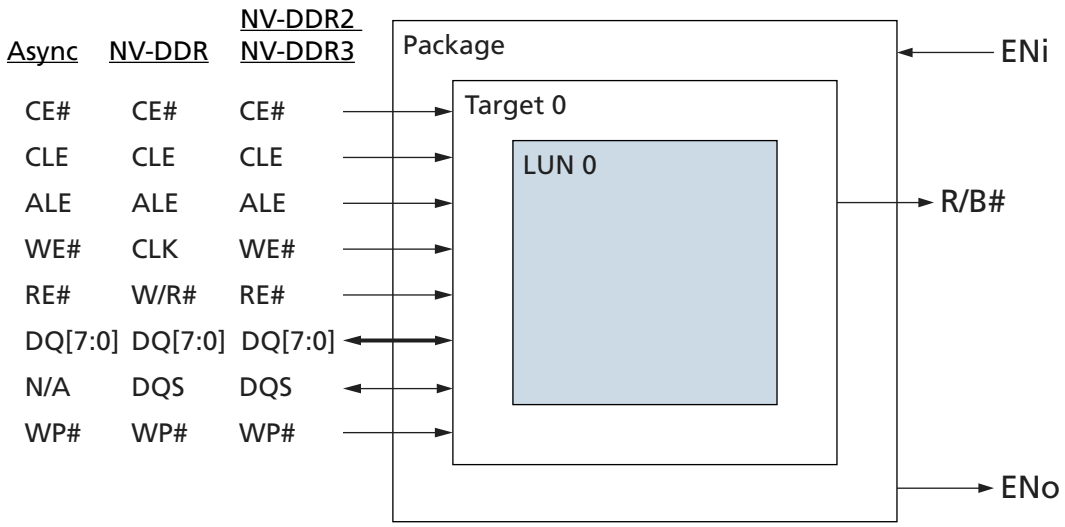


Figure 5: Array Organization per Logical Unit (LUN) for L05B – MLC Mode

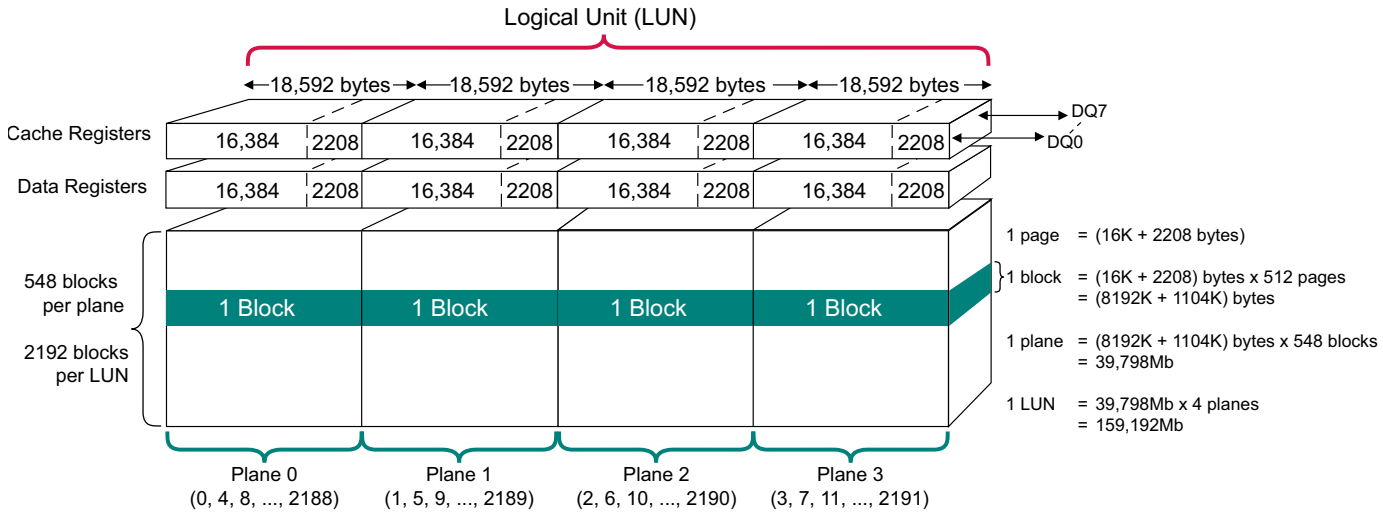


Table 3: Array Addressing for Logical Unit (LUN) for L05B – MLC Mode

Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0[2]
Second	LOW	CA14[3]	CA13	CA12	CA11	CA10	CA9	CA8
Third	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10[4]	BA9[4]	PA8
Fifth	LA2[5, 6]	LA1[5, 6]	LA0[5, 6]	BA20	BA19[5]	BA18	BA17	BA16

Notes:
1. CAx = column address, PAx = page address, BAx = block address, LAx = LUN address; the page address, block address, and LUN address are collectively called the row address.
2. When using the NV-DDR/NV-DDR2 interface, CA0 is forced to 0 internally; one data cycle always returns one even byte and one odd byte.
3. Column addresses 18,592 (48A0h) through 32,767 (7FFFh) are invalid, out of bounds, do not exist in the device, and cannot be addressed.
4. BA[10:9] is the plane-select bit:
   Plane 0: BA[10:9] = 00
   Plane 1: BA[10:9] = 01
   Plane 2: BA[10:9] = 10
   Plane 3: BA[10:9] = 11
5. LA0, LA1, and LA2 are the LUN-select bits. They are present only when two or more LUNs are shared on the target; otherwise, they should be held LOW.
   LUN 0: LA0 = 0, LA1 = 0, LA2 = 0
   LUN 1: LA0 = 1, LA1 = 0, LA2 = 0
   LUN 2: LA0 = 0, LA1 = 1, LA2 = 0
   LUN 3: LA0 = 1, LA1 = 1, LA2 = 0
   LUN 4: LA0 = 0, LA1 = 0, LA2 = 1
   LUN 5: LA0 = 1, LA1 = 0, LA2 = 1
   LUN 6: LA0 = 0, LA1 = 1, LA2 = 1
   LUN 7: LA0 = 1, LA1 = 1, LA2 = 1
6. For single LUN Targets block addresses 2192 through 4095 are invalid, out of bounds, do not exist in the device, and cannot be addressed.
   For two LUN Targets block addresses 2192 through 4095 and 6288 through 8191 are invalid, out of bounds, do not exist in the device, and cannot be addressed.
   For four LUN Targets block addresses 2192 through 4095, 6288 through 8191, 10,384 through 12,287, and 14,480 through 16,383 are invalid, out of bounds, do not exist in the device, and cannot be addressed.
   For eight LUN Targets block addresses 2192 through 4095, 6288 through 8191, 10,384 through 12,287, 14,480 through 16,383, 18,576 through 20,479, 22,672 through 24,575, 26,768 through 28,671, and 30,864 through 32,767 are invalid, out of bounds are invalid, out of bounds, do not exist in the device, and cannot be addressed.

Figure 6: Array Organization per Logical Unit (LUN) for L05B – SLC Mode

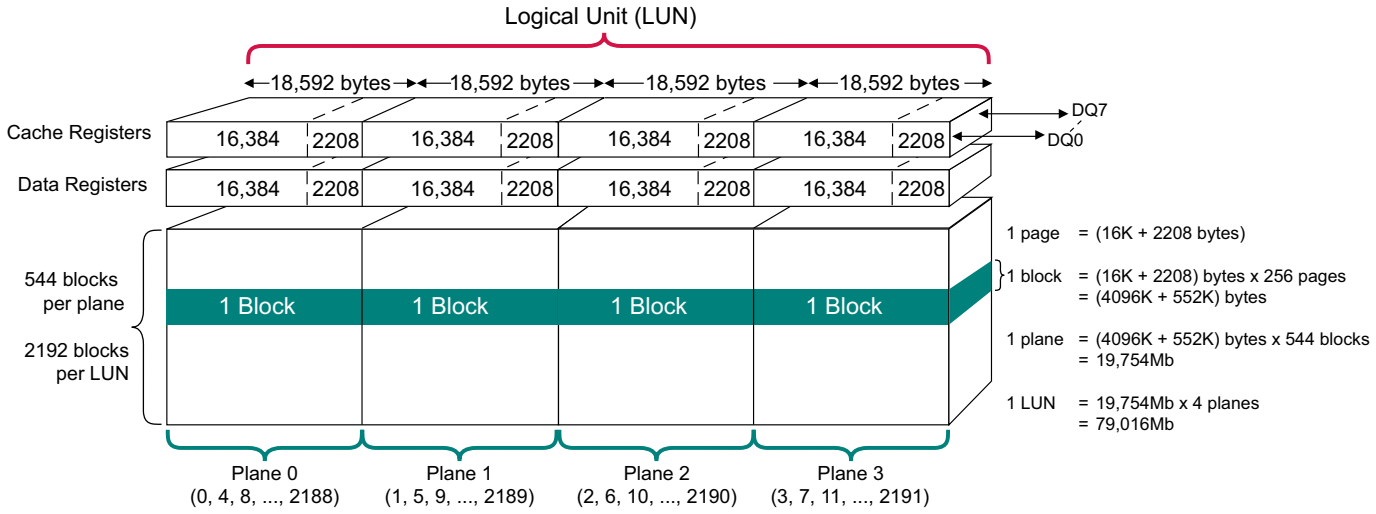


Table 4: Array Addressing for Logical Unit (LUN) for L05B – SLC Mode

Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0[2]
Second	LOW	CA14[3]	CA13	CA12	CA11	CA10	CA9	CA8
Third	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA14	BA13	BA12	BA11	BA10	BA9[4]	BA8[4]	LOW
Fifth	LA2[5, 6]	LA1[5, 6]	LA0[5, 6]	BA19	BA18	BA17	BA16	BA15

Notes:
1. CAx = column address, PAx = page address, BAx = block address, LAx = LUN address; the page address, block address, and LUN address are collectively called the row address.
2. When using the NV-DDR/NV-DDR2 interface, CA0 is forced to 0 internally; one data cycle always returns one even byte and one odd byte.
3. Column addresses 18,592 (48A0h) through 32,767 (7FFFh) are invalid, out of bounds, do not exist in the device, and cannot be addressed.
4. BA[10:9] is the plane-select bit:
   Plane 0: BA[10:9] = 00
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   Plane 2: BA[10:9] = 10
   Plane 3: BA[10:9] = 11
5. LA0, LA1, and LA2 are the LUN-select bits. They are present only when two or more LUNs are shared on the target; otherwise, they should be held LOW.
   LUN 0: LA0 = 0, LA1 = 0, LA2 = 0
   LUN 1: LA0 = 1, LA1 = 0, LA2 = 0
   LUN 2: LA0 = 0, LA1 = 1, LA2 = 0
   LUN 3: LA0 = 1, LA1 = 1, LA2 = 0
   LUN 4: LA0 = 0, LA1 = 0, LA2 = 1
   LUN 5: LA0 = 1, LA1 = 0, LA2 = 1
   LUN 6: LA0 = 0, LA1 = 1, LA2 = 1
   LUN 7: LA0 = 1, LA1 = 1, LA2 = 1
6. For single LUN Targets block addresses 2192 through 4095 are invalid, out of bounds, do not exist in the device, and cannot be addressed.
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For eight LUN Targets block addresses 2192 through 4095, 6288 through 8191, 10,384 through 12,287, 14,480 through 16,383, 18,576 through 20,479, 22,672 through 24,575, 26,768 through 28,671, and 30,864 through 32,767 are invalid, out of bounds are invalid, out of bounds, do not exist in the device, and cannot be addressed.

Bus Operation – Asynchronous Interface

The asynchronous interface is active when the NAND Flash device powers on. The I/O bus, DQ[7:0], is multiplexed sharing data I/O, addresses, and commands. The DQS signal, if present, is tri-stated when the asynchronous interface is active.

Asynchronous interface bus modes are summarized below.

Table 5: Asynchronous Interface Mode Selection

Mode	CE#	CLE	ALE	WE#	RE#	DQS	DQx	WP#	Notes
Standby	H	X	X	X	X	X	X	0V/V_{CCQ}[2]	2
Bus idle	L	X	X	H	H	X	X	X	
Command input	L	H	L		H	X	input	H	
Address input	L	L	H		H	X	input	H	
Data input	L	L	L		H	X	input	H	
Data output	L	L	L	H		X	output	X	
Write protect	X	X	X	X	X	X	X	L	

Notes: 1. DQS is tri-stated when the asynchronous interface is active.
2. WP# should be biased to CMOS LOW or HIGH for standby.
3. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.

Asynchronous Enable/Standby

A chip enable (CE#) signal is used to enable or disable a target. When CE# is driven LOW, all of the signals for that target are enabled. With CE# LOW, the target can accept commands, addresses, and data I/O. There may be more than one target in a NAND Flash package. Each target is controlled by its own chip enable; the first target (Target 0) is controlled by CE#; the second target (if present) is controlled by CE2#, and so forth.

A target is disabled when CE# is driven HIGH, even when the target is busy. When disabled, all of the target's signals are disabled except CE#, WP#, and R/B#. This functionality is also known as CE# “Don't Care”. While the target is disabled, other devices can utilize the disabled NAND signals that are shared with the NAND Flash.

A target enters low-power standby when it is disabled and is not busy. If the target is busy when it is disabled, the target enters standby after all of the die (LUNs) complete their operations. Standby helps reduce power consumption.

Asynchronous Bus Idle

A target's bus is idle when CE# is LOW, WE# is HIGH, and RE# is HIGH.

During bus idle, all of the signals are enabled except DQS, which is not used when the asynchronous interface is active. No commands, addresses, and data are latched into the target; no data is output.

Asynchronous Pausing Data Input/Output

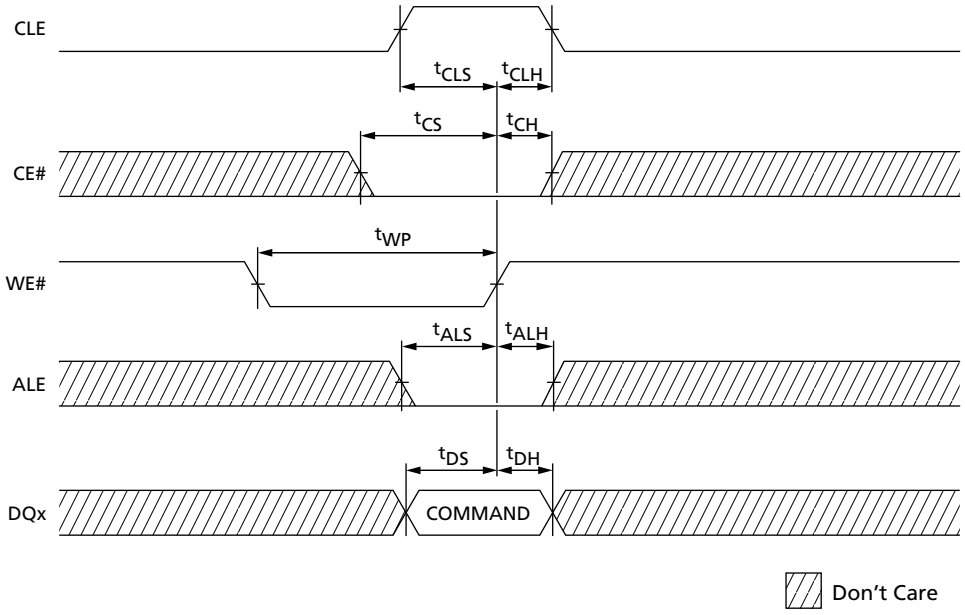
Pausing data input or data output is done by keeping WE# or RE# HIGH, respectively.

Asynchronous Commands

An asynchronous command is written from DQ[7:0] to the command register on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is HIGH, and RE# is HIGH.

Commands are typically ignored by die (LUNs) that are busy (RDY = 0); however, some commands, including READ STATUS (70h) READ STATUS ENHANCED (78h), and FIXED ADDRESS READ STATUS ENHANCED (71h) are accepted by die (LUNs) even when they are busy.

Figure 7: Asynchronous COMMAND LATCH Cycle



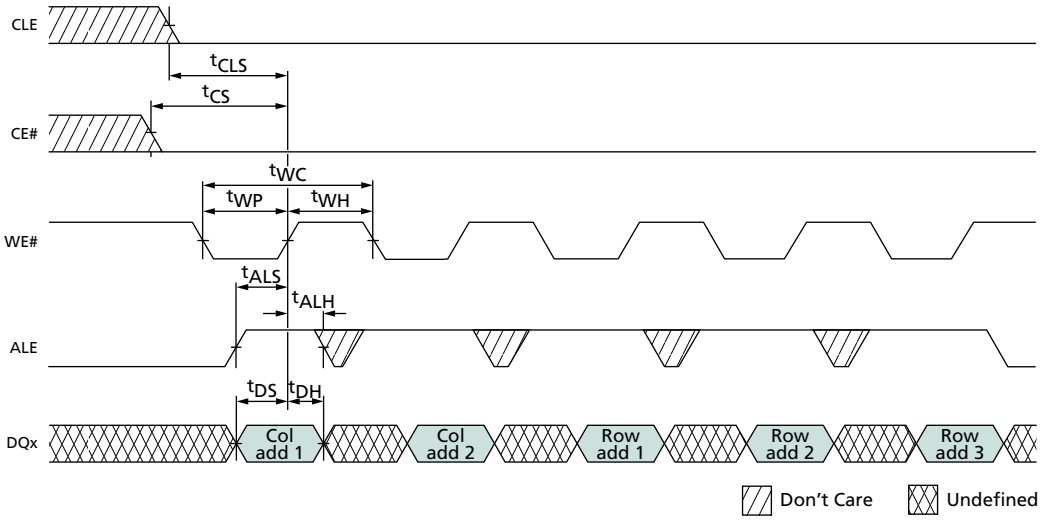
Asynchronous Addresses

An asynchronous address is written from DQ[7:0] to the address register on the rising edge of WE# when CE# is LOW, ALE is HIGH, CLE is LOW, and RE# is HIGH.

Bits that are not part of the address space must be LOW (see Device and Array Organization). The number of cycles required for each command varies. Refer to the command descriptions to determine addressing requirements (see Command Definitions).

Addresses are typically ignored by die (LUNs) that are busy (RDY = 0); however, some addresses are accepted by die (LUNs) even when they are busy; for example, address cycles that follow the READ STATUS ENHANCED (78h) command.

Figure 8: Asynchronous ADDRESS LATCH Cycle

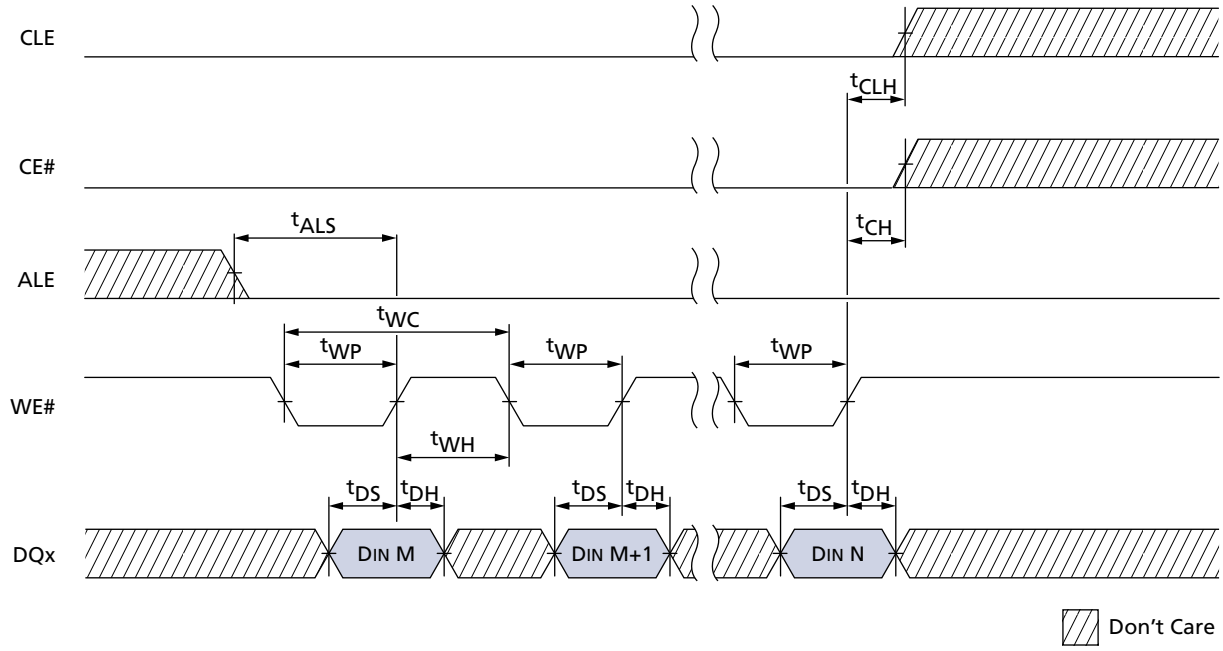


Asynchronous Data Input

Data is written from DQ[7:0] to the cache register of the selected die (LUN) on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is LOW, and RE# is HIGH.

Data input is ignored by die (LUNs) that are not selected or are busy (RDY = 0).

Figure 9: Asynchronous Data Input Cycles



Asynchronous Data Output

Data can be output from a die (LUN) if it is in a READY state. Data output is supported following a READ operation from the NAND Flash array. Data is output from the cache register of the selected die (LUN) to DQ[7:0] on the falling edge of RE# when CE# is LOW, ALE is LOW, CLE is LOW, and WE# is HIGH.

If the host controller is using a ^{t}RC of 30ns or greater, the host can latch the data on the rising edge of RE# (see Figure 10). If the host controller is using a ^{t}RC of less than 30ns, the host can latch the data on the next falling edge of RE# [see Figure 11 for extended data output (EDO) timing].

Using the READ STATUS ENHANCED (78h) or the FIXED ADDRESS READ STATUS ENHANCED (71h) command prevents data contention following an interleaved die (multi-LUN) operation. After issuing the READ STATUS ENHANCED (78h) command, to enable data output, issue the READ MODE (00h) command.

Data output requests are typically ignored by a die (LUN) that is busy (RDY = 0); however, it is possible to output data from the status register even when a die (LUN) is busy by first issuing the READ STATUS (70h) or READ STATUS ENHANCED (78h) or FIXED ADDRESS READ STATUS ENHANCED (71h) command.

Figure 10: Asynchronous Data Output Cycles

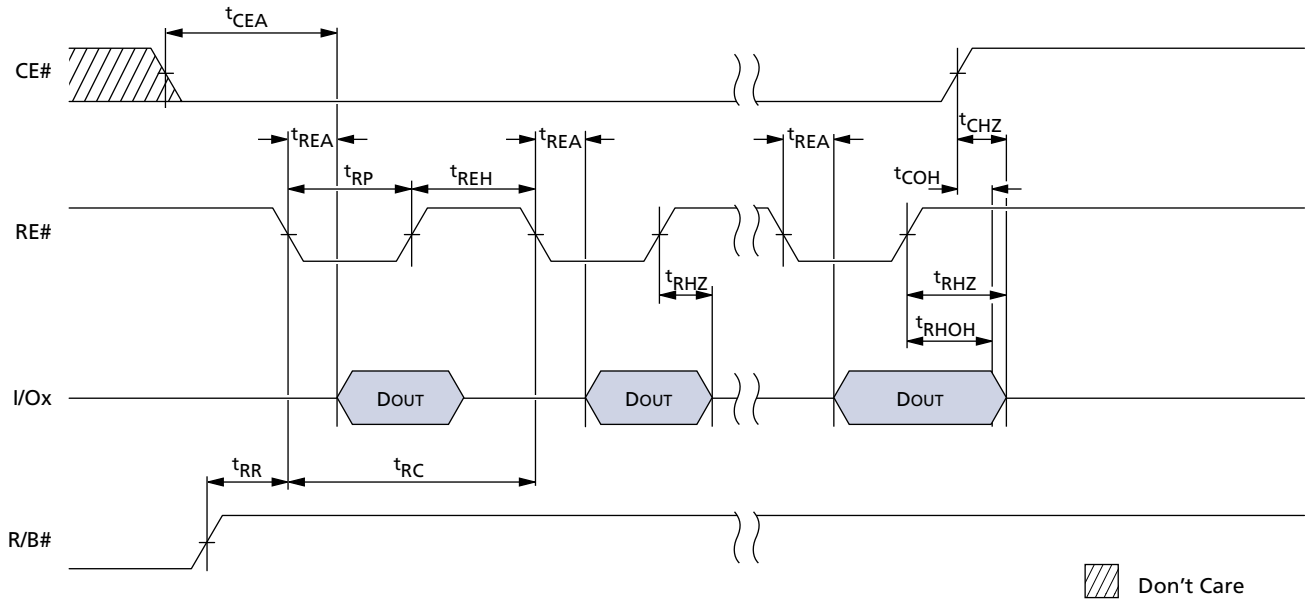
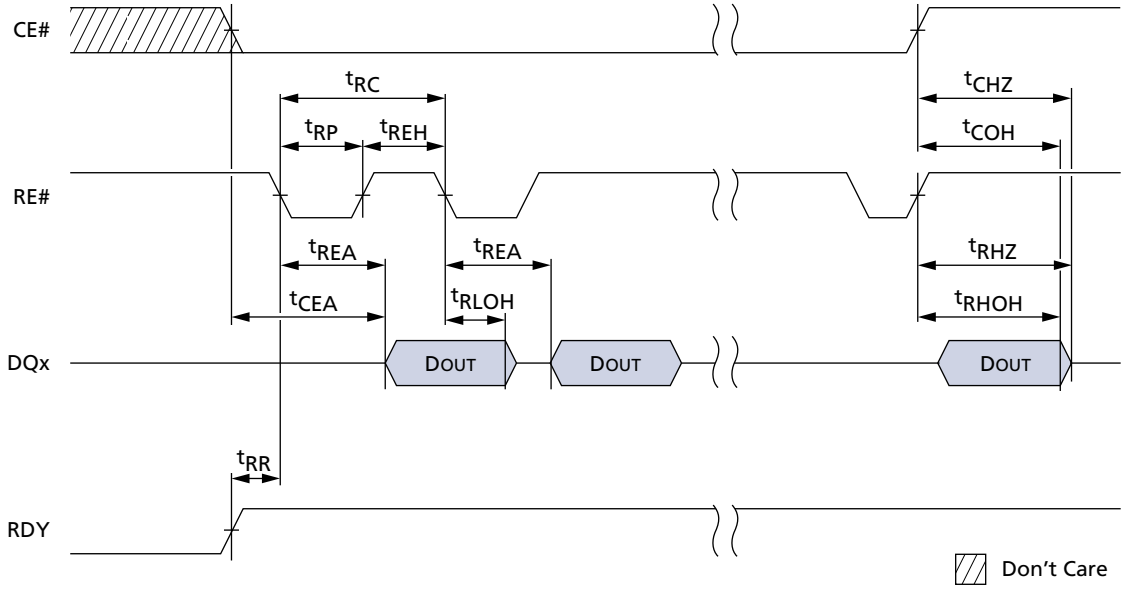


Figure 11: Asynchronous Data Output Cycles (EDO Mode)



Write Protect (WP#)

The WP# signal enables or disables PROGRAM and ERASE operations to a target. When WP# is LOW, PROGRAM and ERASE operations are disabled. When WP# is HIGH, PROGRAM and ERASE operations are enabled.

It is recommended that the host drive WP# LOW during power-on until V_{CC} and V_{CCQ} are stable to prevent inadvertent PROGRAM and ERASE operations (see V_{CC} Power Cycling for additional details).

WP# must be transitioned only when the target is not busy and prior to beginning a command sequence. After a command sequence is complete and the target is ready, WP# can be transitioned. After WP# is transitioned the host must wait ^{t}WW before issuing a new command.

The WP# signal is always an active input, even when CE# is HIGH. This signal should not be multiplexed with other signals.

Ready/Busy# (R/B#)

The ready/busy# (R/B#) signal provides a hardware method of indicating whether a target is ready or busy. A target is busy when one or more of its die (LUNs) are busy (RDY = 0). A target is ready when all of its die (LUNs) are ready (RDY = 1). Because each die (LUN) contains a status register, it is possible to determine the independent status of each die (LUN) by polling its status register instead of using the R/B# signal (see Status Operations for details regarding LUN status).

This signal requires a pull-up resistor, Rp, for proper operation. R/B# is HIGH when the target is ready, and transitions LOW when the target is busy. The signal's open-drain driver enables multiple R/B# outputs to be OR-tied. Typically, R/B# is connected to an interrupt pin on the system controller (see Figure 12).

It is not permitted to drive or have the NAND R/B# signal HIGH while the NAND V_{CCQ} voltage is below V_{CCQ} Min.

The combination of Rp and capacitive loading of the R/B# circuit determines the rise time of the R/B# signal. The actual value used for Rp depends on the system timing requirements. Large values of RP cause R/B# to be delayed significantly. Between the 10- to 90-percent points on the R/B# waveform, the rise time is approximately two time constants (TC).

$$TC = R \times C$$

Where R = *Rp* (resistance of pull-up resistor), and C = total capacitive load.

The fall time of the R/B# signal is determined mainly by the output impedance of the R/B# signal and the total load capacitance. Approximate Rp values using a circuit load of 100pF are provided in Figure 13.

The minimum value for Rp is determined by the output drive capability of the R/B# signal, the output voltage swing, and V_{CCQ}.

$$Rp = \frac{VCC(MAX) - VOL(MAX)}{IOL + \Sigma IL}$$

Where ΣIL is the sum of the input currents of all devices tied to the R/B# pin.

Figure 12: READ/BUSY# Open Drain

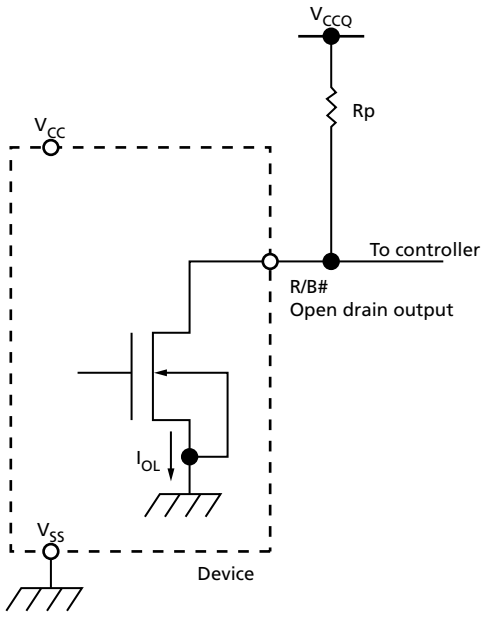
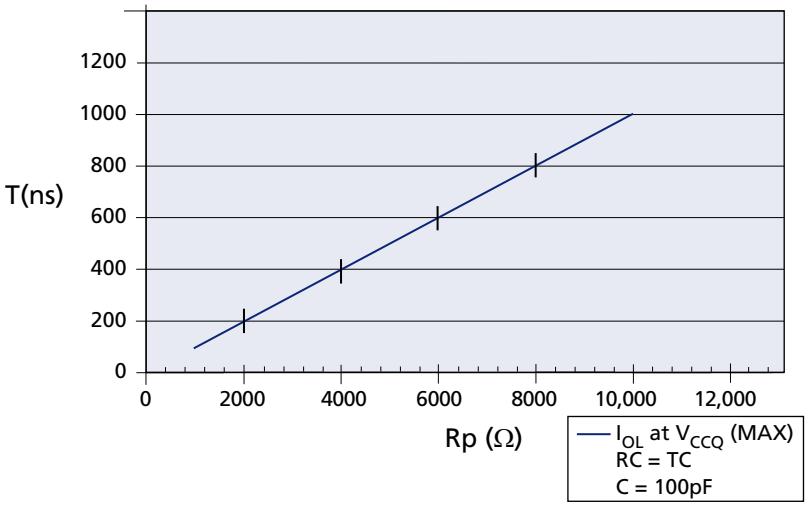


Figure 13: TC vs Rp



Bus Operation – NV-DDR Interface

The NAND Flash command protocol for both the asynchronous and NV-DDR interfaces is identical. However, there are some differences between the asynchronous and NV-DDR interfaces when issuing command, address, and data I/O cycles using the NAND Flash signals.

When the NV-DDR interface is activated on a target (see Activating Interfaces), the target is capable of high-speed NV-DDR data transfers. Existing signals are redefined for high-speed NV-DDR I/O. The WE# signal becomes CLK. DQS is enabled. The RE# signal becomes W/R#. CLK provides a clock reference to the NAND Flash device.

DQS is a bidirectional data strobe. During data output, DQS is driven by the NAND Flash device. During data input, DQS is controlled by the host controller while inputting data on DQ[7:0].

The direction of DQS and DQ[7:0] is controlled by the W/R# signal. When the W/R# signal is latched HIGH, the controller is driving the DQ bus and DQS. When the W/R# is latched LOW, the NAND Flash is driving the DQ bus and DQS.

Transition from the NV-DDR interface to the NV-DDR2 interface is not permitted.

The NV-DDR interface bus modes are summarized below.

Table 6: NV-DDR Interface Mode Selection

Mode	CE#	CLE	ALE	CLK	W/R#	DQS	DQ[7:0]	WP#	Notes
Standby	H	X	X	X	X	X	X	0V/V_{CCQ}	1, 2
Bus idle	L	L	L	⌐↑	H	X	X	X	
Bus driving	L	L	L	⌐↑	L	output	output	X	
Command input	L	H	L	⌐↑	H	X	input	H	3
Address input	L	L	H	⌐↑	H	X	input	H	3
Data input	L	H	H	↑↓	H	↑↓	input	H	4
Data output	L	H	H	↑↓	L	note 5	output	X	5
Write protect	X	X	X	X	X	X	X	L	
Undefined	L	L	H	⌐↑	L	output	output	X	
Undefined	L	H	L	⌐↑	L	output	output	X	

Notes:
1. CLK can be stopped when the target is disabled, even when R/B# is LOW.
2. WP# should be biased to CMOS LOW or HIGH for standby.
3. Commands and addresses are latched on the rising edge of CLK.
4. During data input to the device, DQS is the “clock” that latches the data in the cache register.
5. During data output from the NAND Flash device, DQS is an output generated from CLK after ^{t}DQSCK delay.

6. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.

NV-DDR Enable/Standby

In addition to the description found in Asynchronous Enable/Standby, the following requirements also apply when the synchronous interface is active.

Before enabling a target, CLK must be running and ALE and CLE must be LOW. When CE# is driven LOW, all of the signals for the selected target are enabled. The target is not enabled until ^{t}CS completes; the target's bus is then idle.

Prior to disabling a target, the target's bus must be idle. A target is disabled when CE# is driven HIGH, even when it is busy. All of the target's signals are disabled except CE#, WP#, and R/B#. After the target is disabled, CLK can be stopped.

A target enters low-power standby when it is disabled and is not busy. If the target is busy when it is disabled, the target enters standby after all of the LUNs complete their operations.

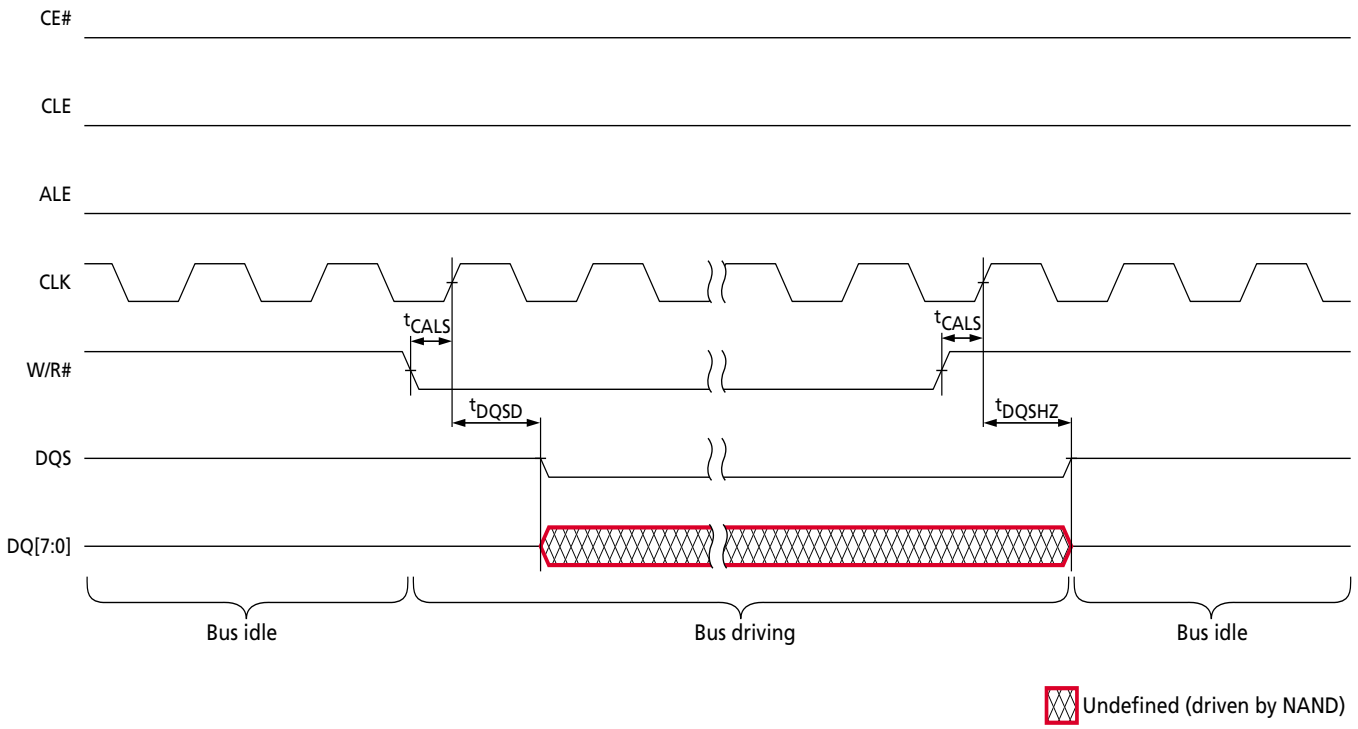
NV-DDR Bus Idle/Driving

A target's bus is idle or driving when CLK is running, CE# is LOW, ALE is LOW, and CLE is LOW.

The bus is idle when W/R# transitions HIGH and is latched by CLK. During the bus idle mode, all signals are enabled; DQS and DQ[7:0] are inputs. No commands, addresses, or data are latched into the target; no data is output. When entering the bus idle mode, the host must wait a minimum of ^{t}CAD before changing the bus mode. In the bus idle mode, the only valid bus modes supported are: bus driving, command, address, and NV-DDR data input.

The bus is driving when W/R# transitions LOW and is latched by CLK. During the bus driving mode, all signals are enabled; DQS is LOW and DQ[7:0] is driven LOW or HIGH, but no valid data is output. Following the bus driving mode, the only valid bus modes supported are bus idle and NV-DDR data output.

Figure 14: NV-DDR Bus Idle/Driving Behavior



Notes: 1. Only the selected die (LUN) drives DQS and DQ[7:0]. During an interleaved die (multi-LUN) operation, the host must use the READ STATUS ENHANCED (78h) to prevent data output contention.

NV-DDR Pausing Data Input/Output

Pausing data input or data output is done by setting ALE and CLE to LOW. The host may continue data transfer by setting ALE and CLE to HIGH after the applicable ^{t}CAD time has passed.

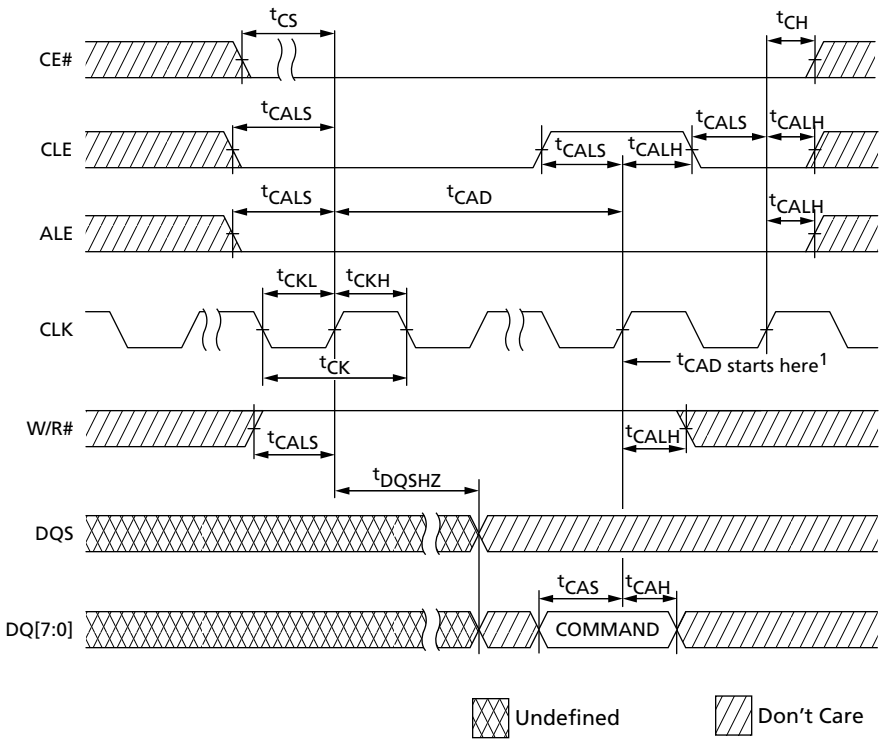
NV-DDR Commands

A command is written from DQ[7:0] to the command register on the rising edge of CLK when CE# is LOW, ALE is LOW, CLE is HIGH, and W/R# is HIGH.

After a command is latched, and prior to issuing the next command, address, or data I/O, the bus must go to the bus idle mode on the next rising edge of CLK, except when the clock period, ^{t}CK, is greater than ^{t}CAD.

Commands are typically ignored by LUNs that are busy (RDY = 0); however, some commands, such as READ STATUS (70h) and READ STATUS ENHANCED (78h), are accepted by LUNs, even when they are busy.

Figure 15: NV-DDR Command Cycle



Notes: 1. When CE# remains LOW, ^{t}CAD begins at the rising edge of the clock from which the command cycle is latched for subsequent command, address, data input, or data output cycle(s).

NV-DDR Addresses

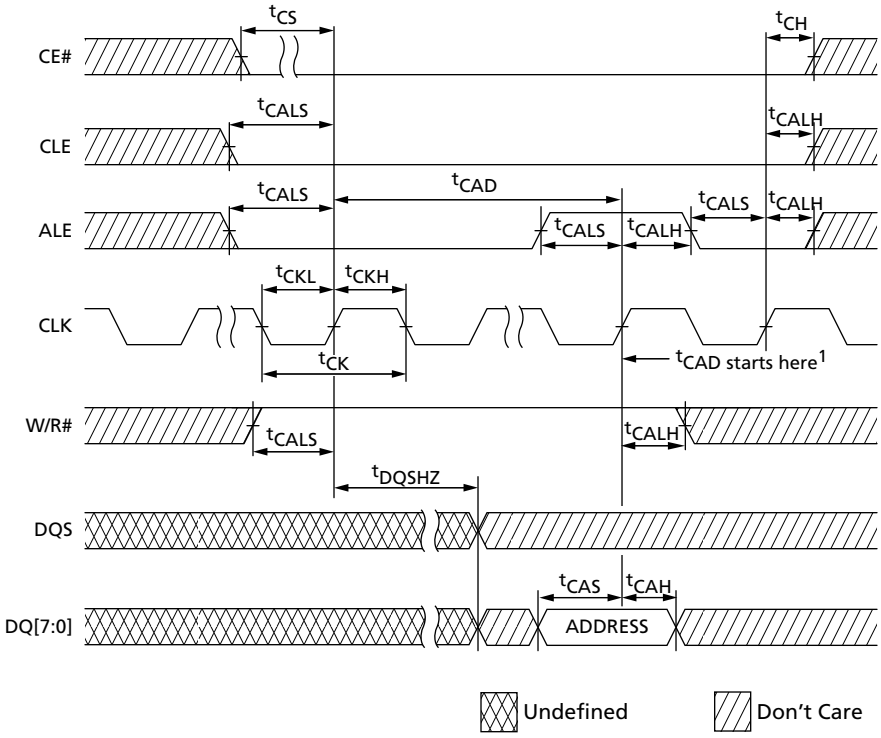
A NV-DDR address is written from DQ[7:0] to the address register on the rising edge of CLK when CE# is LOW, ALE is HIGH, CLE is LOW, and W/R# is HIGH.

After an address is latched, and prior to issuing the next command, address, or data I/O, the bus must go to the bus idle mode on the next rising edge of CLK, except when the clock period, ^{t}CK, is greater than ^{t}CAD.

Bits not part of the address space must be LOW (see Device and Array Organization). The number of ADDRESS cycles required for each command varies. Refer to the command descriptions to determine addressing requirements.

Addresses are typically ignored by LUNs that are busy (RDY = 0); however, some addresses such as address cycles that follow the READ STATUS ENHANCED (78h) command, are accepted by LUNs, even when they are busy.

Figure 16: NV-DDR Address Cycle



Notes: 1. When CE# remains LOW, tCAD begins at the rising edge of the clock from which the command cycle is latched for subsequent command, address, data input, or data output cycle(s).

NV-DDR DDR Data Input

To enter the NV-DDR data input mode, the following conditions must be met:

- CLK is running,
- CE# is LOW,
- W/R# is HIGH,
- tCAD is met,
- DQS is LOW, and
- ALE and CLE are HIGH on the rising edge of CLK.

Upon entering the NV-DDR data input mode after tDQSS, data is written from DQ[7:0] to the cache register on each and every rising and falling edge of DQS (center-aligned) when CLK is running and the DQS to CLK skew meets tDSH and tDSS, CE# is LOW, W/R# is HIGH, and ALE and CLE are HIGH on the rising edge of CLK.

To exit NV-DDR data input mode, the following conditions must be met:

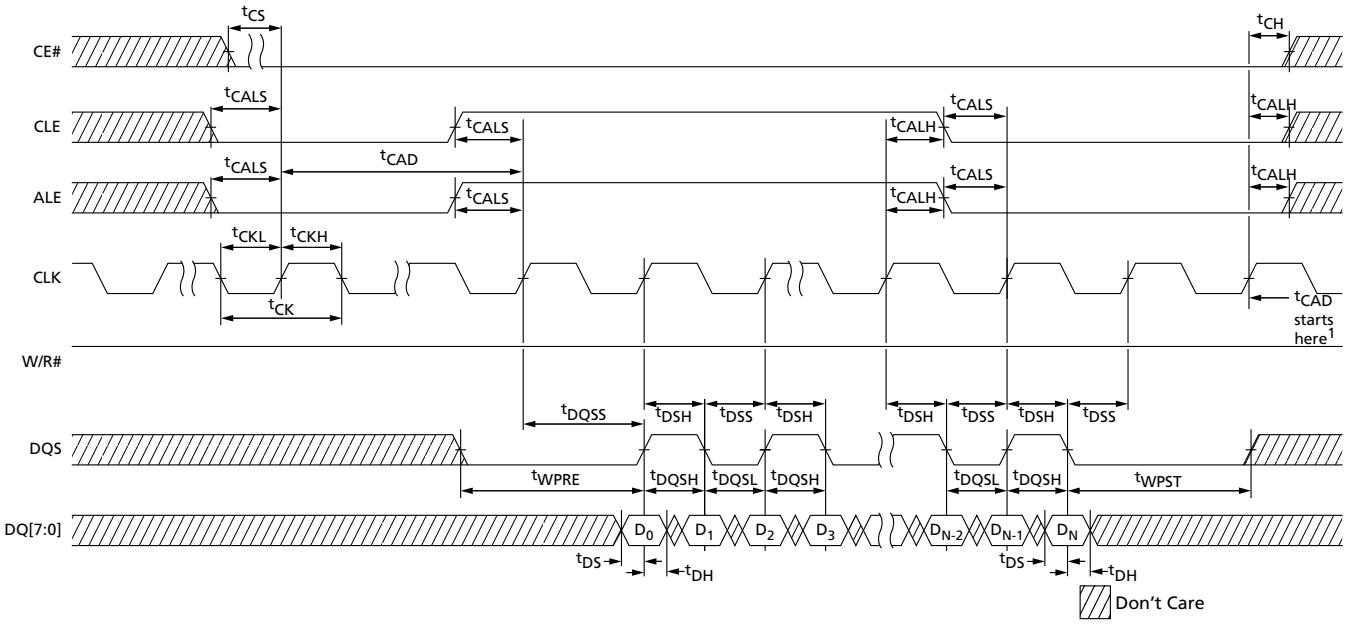
- CLK is running and the DQS to CLK skew meets tDSH and tDSS,
- CE# is LOW,
- W/R# is HIGH
- ALE and CLE are HIGH on the rising edge of CLK.
- The final two data bytes of the data input sequence are written from DQ[7:0] to the cache register on the final rising and falling edges of DQS after the last cycle in the data input sequence ALE and CLE are latched HIGH, and

- DQS is held LOW for tWPST (after the final falling edge of DQS).

Following tWPST, the bus enters bus idle mode and tCAD begins on the next rising edge of CLK. After tCAD starts, the host can disable the target if desired.

Data input is ignored by LUNs that are not selected or are busy.

Figure 17: NV-DDR Data Input Cycles



Notes: 1. When CE# remains LOW, tCAD begins at the first rising edge of the clock after tWPST completes.
2. tDSH (MIN) generally occurs during tDQSS (MIN).
3. tDSS (MIN) generally occurs during tDQSS (MAX).

NV-DDR Data Output

Data can be output from a die (LUN) if it is ready. Data output is supported following a READ operation from the NAND Flash array.

To enter the NV-DDR data output mode, the following conditions must be met:

- CLK is running
- CE# is LOW
- The host has released the DQ[7:0] bus and DQS
- W/R# is latched LOW on the rising edge of CLK to enable the selected LUN to take ownership of the DQ[7:0] bus and DQS within tWRCK
- tCAD is met, and
- ALE and CLE are HIGH on the rising edge of CLK.

Upon entering the NV-DDR data output mode, DQS will toggle HIGH and LOW with a delay of tDQSCK from the respective rising and falling edges of CLK. DQ[7:0] will output data edge-aligned to the rising and falling edges of DQS, with the first transition delayed by no more than tAC.

NV-DDR data output mode continues as long as CLK is running, CE# is LOW, W/R# is LOW, and ALE and CLE are HIGH on the rising edge of CLK.

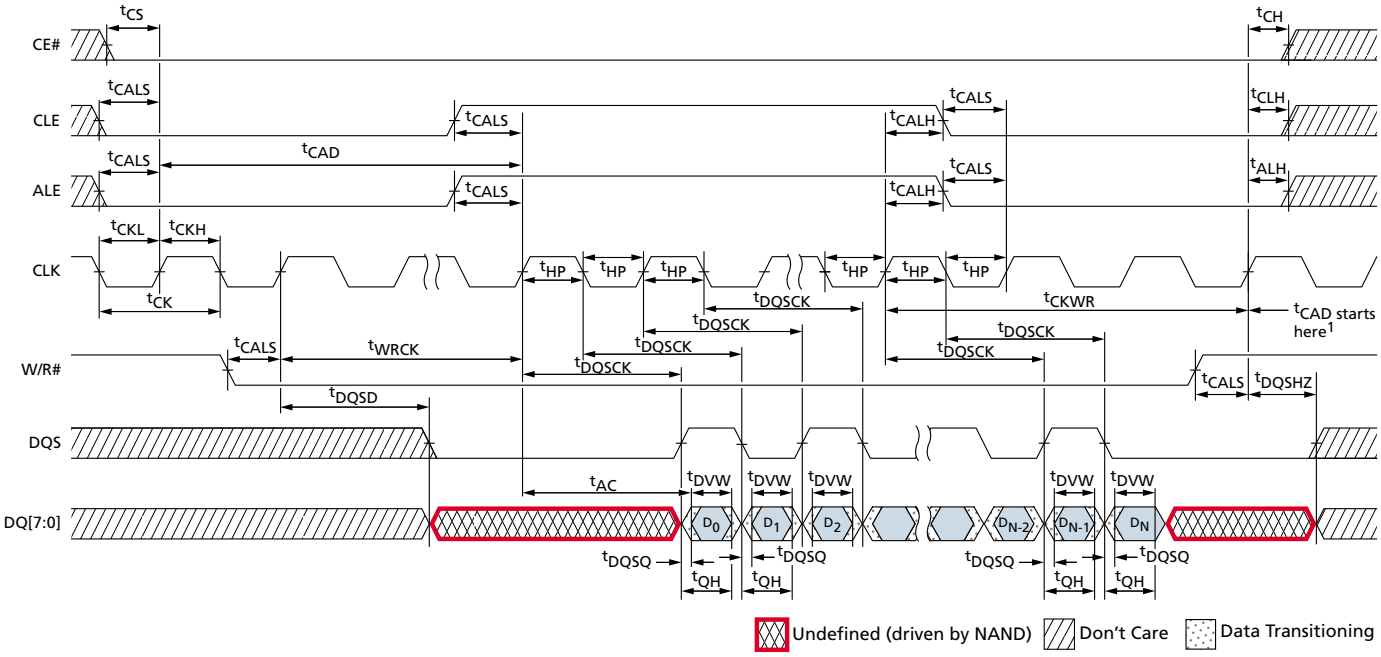
To exit NV-DDR data output mode, the following conditions must be met:

- CLK is running
- CE# is LOW
- W/R# is LOW
- ALE and CLE are HIGH on the rising edge of CLK

The final two data bytes will be output on DQ[7:0] on the final rising and falling edges of DQS. The final rising and falling edges of DQS occur ^{t}DQSCK after the last cycle in the data output sequence where ALE and CLE are latched HIGH. Following ^{t}CKWR, the bus enters bus idle mode, and ^{t}CAD begins on the next rising edge of CLK. After ^{t}CAD starts, the host can disable the target if desired.

Data output requests are typically ignored by a LUN that is busy; however, it is possible to output data from the status register even when a LUN is busy by issuing the READ STATUS or READ STATUS ENHANCED (78h) command.

Figure 18: NV-DDR Data Output Cycles



Notes:
1. When CE# remains LOW, ^{t}CAD begins at the rising edge of the clock after ^{t}CKWR for subsequent command or data output cycle(s).
2. See Figure 15 for details of W/R# behavior.
3. ^{t}AC is the DQ output window relative to CLK and is the long-term component of DQ skew.
4. For W/R# transitioning HIGH: DQ[7:0] and DQS go to tri-state.
5. For W/R# transitioning LOW: DQ[7:0] drives current state and DQS goes LOW.
6. After final data output, DQ[7:0] is driven until W/R# goes HIGH, but is not valid.

Write Protect

See Write Protect under Bus Operation – Asynchronous Interface.

Ready/Busy#

See Ready Busy under Bus Operation – Asynchronous Interface.

Bus Operation – NV-DDR2 Interface

When the NV-DDR2 interface is activated on a target (see Activating Interfaces), the target is capable of high-speed DDR data transfers. and the DQS signal is enabled. DQS is a bidirectional data strobe. During data output, DQS is driven by the NAND Flash device. During data input, DQS is controlled by the host controller while inputting data on DQ[7:0].

For operations in NV-DDR2 mode, the NV-DDR2 interface must be selected (see Activating the NV-DDR2 Interface). The capabilities that NV-DDR2 operations offers beyond NV-DDR operations include:

- Supported only at 1.8V V_{CCQ}
- Support for speeds beyond 200MT/s
- Support for differential signaling for the RE# and/or DQS signals (RE_c, DQS_c)
- Support for Warmup Cycles
- Support for On-die Termination (ODT)
- Support for V_{REFQ}

Use of differential signaling and external V_{REFQ} is optional for interface speeds 200 MT/s or slower. Differential signaling and external V_{REFQ} are optional for NV-DDR2 interface speeds faster than 200 MT/s but required to guarantee specified AC timings. If a host does not use differential signaling and external V_{REFQ} at speeds faster than 200 MT/s, specified AC timings are not guaranteed. If not using the differential signaling, statements about those signal types can be ignored.

Transition from the NV-DDR2 interface to the NV-DDR interface is not permitted.

The NV-DDR2 interface bus modes are summarized below:

Table 7: NV-DDR2 Interface Mode Selection

Mode	CE#	CLE	ALE	RE# (RE_t)	DQS (DQS_t)	DQ[7:0][1]	WE#	WP#	Notes
Standby	H	X	X	X	X	X	X	0V/V_{CCQ}	1, 2
Idle	L	L	L	H	H	X	H	X	6
Command input	L	H	L	H	H	input		H	3
Address input	L	L	H	H	X[4]	input		H	3
Data input	L	L	L	H		input	H	H	2, 3
Data output	L	L	L			output	H	X	2, 3, 5
Write protect	X	X	X	X	X	X	X	L	

Notes: 1. The current state of the device is data input, data output, or neither based on the commands issued.
2. There are two data input/output cycles from the rising edge of DQS/RE# to the next rising edge of DQS/RE#.
3. ODT may be enabled as part of the data input and data output cycles.

4. When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.
5. At the beginning of the data output burst, DQS shall be held HIGH for ^{t}DQSRH after RE# transitions LOW to begin data output. ^{t}DQSRH is only required if Matrix ODT is enabled.
6. WE# is set HIGH during the idle state.
7. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.

Differential Signaling

An enabler for higher speed operation is differential signaling for the RE# and DQS signals. A complementary RE# and complementary DQS signal may be optionally used to create differential signal pairs (RE_t/RE_c and DQS_t/DQS_c). When using differential signaling, RE# is referred to as RE_t and DQS is referred to as DQS_t, for example, the "true" versions of the signals. Differential signaling may be used to improve signal integrity through enhanced noise immunity. Differential signaling shall only be enabled for use when the NV-DDR2 data interface is selected.

A device may support differential RE# and/or differential DQS signaling. The support for differential RE# and/or DQS is reported in the parameter page. Complementary RE# (for example, RE_c) and complementary DQS (for example, DQS_c) signals are individually configured/enabled. By default, differential signaling is disabled. The host may configure the device to use differential signaling using the NV-DDR2 Configuration feature address.

Differential signaling is not enabled by default. It is recommended that if differential signaling is used by a host system that is it enabled at the same time as the interface utilizing the differential signaling is enabled.

To begin using differential signaling, the host shall issue a SET FEATURES (EFh) command to the Timing Mode feature address that sets the Data Interface from asynchronous to NV-DDR2 operation. Then issue a SET FEATURES (EFh) command to the NV-DDR2 Configuration feature address to activate differential RE# and/or differential DQS signaling. The differential signaling is then enabled after CE# is brought HIGH.

To change from differential signaling to single-ended signaling, the host shall configure the device using the NV-DDR2 Configuration feature address to disable differential signaling. The differential signaling is disabled after CE# is brought HIGH.

A RESET (FFh) command will disable differential signaling. The SYNCHRONOUS RESET (FCh) and RESET LUN (FAh) commands have no effect on differential signaling.

Warmup Cycles

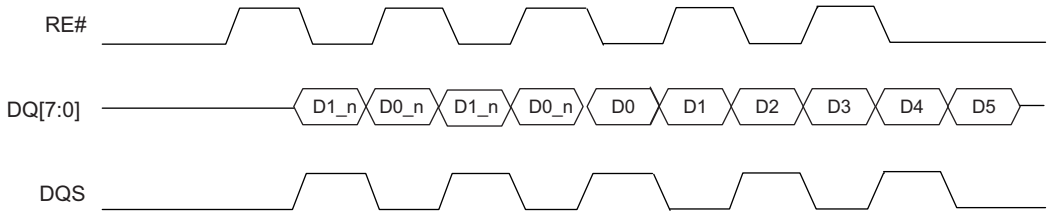
In order to support higher speed operation, WARMUP cycles for data output and data input may be provided. WARMUP cycles shall only be enabled for use when the NV-DDR2 data interface is selected.

WARMUP cycles for data output provides extra RE# and corresponding DQS transitions at the beginning of a data output burst. These extra RE#/DQS transitions do not have any data associated with them. The number of extra cycles is configured via the NV-DDR2 configuration feature address.

WARMUP cycles for data input provides extra DQS transitions at the beginning of a data input burst. These extra DQS transitions do not have any data associated with them. The number of extra cycles is configured via the NV-DDR2 Configuration feature address. The number of cycles specified includes a full data input cycle (both rising and falling edge for DQS).

WARMUP cycles are optional for both data output and data input, and if used, do not need to be configured to the same value. WARMUP cycles apply to all commands. WARMUP cycles are initiated at the start of each data burst when WARMUP cycles are enabled for that data transfer type. If the host pauses and then resumes a data transfer without exiting and re-entering the data burst, then the host shall not issue additional WARMUP cycles. Exiting and re-entering the data burst shall be performed by bringing ALE, CLE, or CE# HIGH without latching with WE#. In the case of not re-issuing WARMUP cycles, the host should take care to avoid signal integrity issues due to pausing the data transfer and resuming without WARMUP cycles.

Figure 19: Warmup Cycles for data output (2 warmup cycles)



On-die Termination (ODT)

On-die termination (ODT) may be required at higher speeds depending on system topology. ODT applies to the DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c signals. ODT is an optional capability that may be employed to meet higher speeds in particular topologies. If power needs to be optimized in a particular condition, then ODT may be disabled and the topology may be run at a slower timing mode. ODT shall only be enabled for use in the NV-DDR2 data interface.

ODT settings are configured during device initialization. The host may configure the ODT in a self-termination only configuration, or matrix termination which enables a combination of target and non-target termination to be specified.

For the more flexible matrix termination the host configures a matrix that defines the LUN(s) that terminate for a particular volume. This matrix is configured using the ODT CONFIGURE (E2h) command. After the ODT matrix is defined, ODT is enabled and disabled based on the type of cycle (on for data input and output cycles, off for command, and address cycles). ODT applies for data input and output cycles for all command types, including both single data rate (SDR) and double data rate (DDR) transfers.

Volume addressing is required for use of non-target ODT functionality. See Configuration Operations for how to appoint volume addresses. Once volume addresses have been appointed they can be selected with the VOLUME SELECT (E1h) command. For target only termination, no ODT termination matrix is required.

The ODT configuration matrix and control mechanism utilize volume addresses. Volume addressing is a required capability to utilize non-target ODT.

The ODT settings are retained across RESET (FAh, FCh, FFh) commands, but are not retained across HARD RESET (FDh) commands for the target LUN.

When ODT is enabled via the NV-DDR2 Configuration feature address, the default is target termination. For non-target termination or termination topologies that use multiple terminators, the volume address mechanism shall be used and the ODT configuration matrix shall be specified using the ODT CONFIGURE (E2h) command. As part of the ODT CONFIGURE (E2h) command, R_{TT} settings may be specified on a per LUN basis with individual values for:

- RE#
- DQ[7:0] and DQS for data output
- DQ[7:0] and DQS for data input

Table 8: On-die Termination DC Electrical Characteristics

Mode	Symbol	Min	Max	Units	Notes
R_{TT} effective impedance value for 50 Ohm setting	$R_{TT2(EFF)}$	32.5	67.5	Ohms	1
R_{TT} effective impedance value for 75 Ohm setting	$R_{TT3(EFF)}$	48.7	101.3	Ohms	1
R_{TT} effective impedance value for 100 Ohm setting	$R_{TT4(EFF)}$	65	135	Ohms	1
R_{TT} effective impedance value for 150 Ohm setting	$R_{TT5(EFF)}$	97.5	202.5	Ohms	1
Deviation of VM with respective to $V_{CCQ}/2$	ΔVM	-7	7	Percent	2

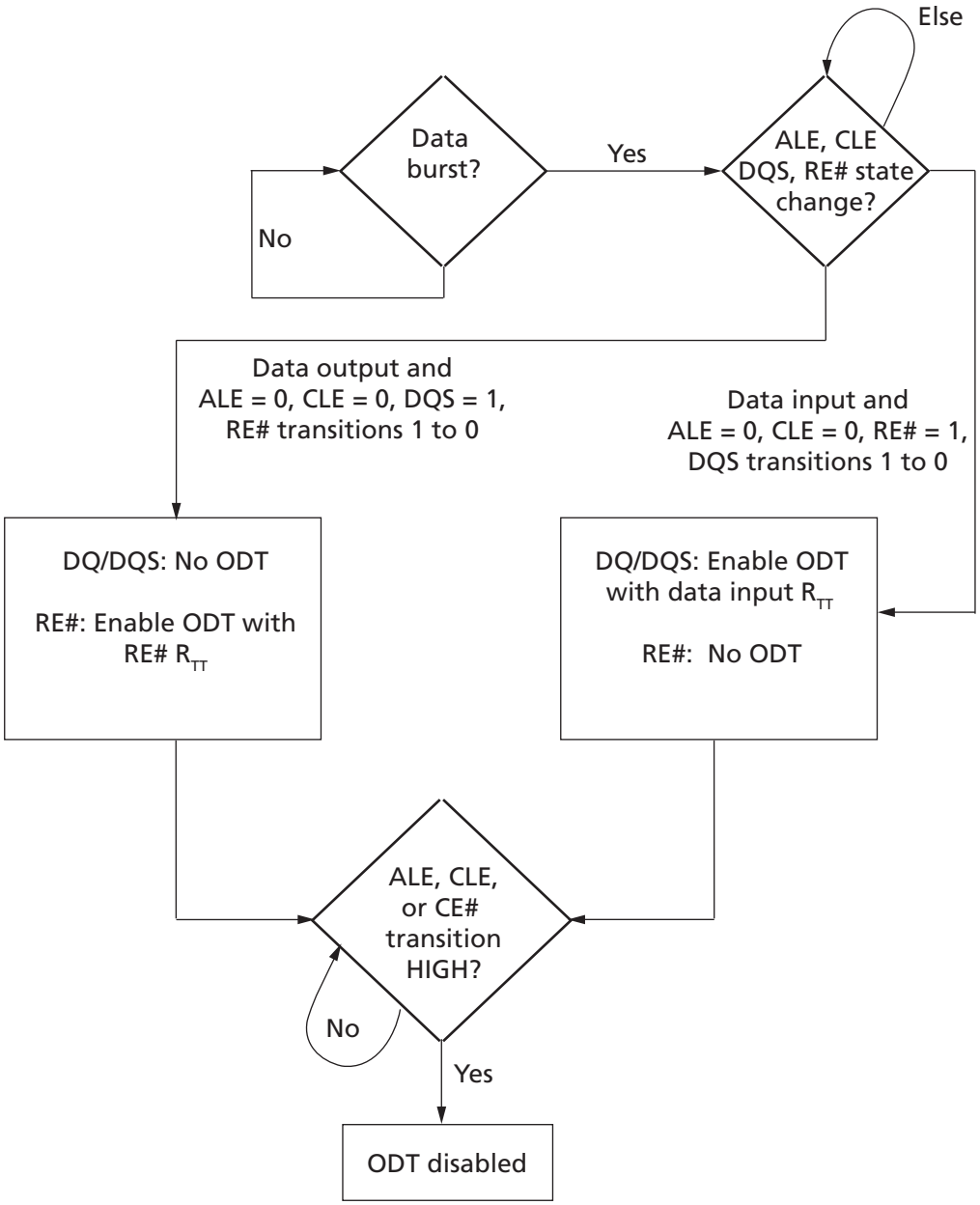
Notes: 1. $R_{TT2(EFF)}$, $R_{TT3(EFF)}$, $R_{TT4(EFF)}$, and $R_{TT5(EFF)}$ are determined by separately applying $V_{IH(AC)}$ and $V_{IL(AC)}$ to the signal being tested, and then measuring current $I(V_{IH[AC]})$ and $I(V_{IL[AC]})$, respectively. $R_{TT(EFF)} = (V_{IH[AC]}) – (V_{IL[AC]}) / I(V_{IH[AC]}) – I(V_{IL[AC]})$
2. Measure voltage (VM) at the tested signal with no load. $\Delta VM = [(2 \times VM) / V_{CCQ}] \times 100$.

Self-termination On-die Termination (ODT)

When self-termination is enabled, the LUN that is executing the command provides on-die termination. Figure 20 on page 38 defines the self-termination only ODT enable and disable requirements for the LUN that is executing the command when ODT is selected for use via SET FEATURES (EFh) command. If the ODT CONFIGURE (E2h) command is issued to a LUN on a Target, then the ODT mechanism used for that Target changes to matrix termination.

Self-termination is applied to DQS and DQ[7:0] signals during data input operations and RE# during data output operations.

Figure 20: Self-termination only ODT behavioral flow



Matrix Termination

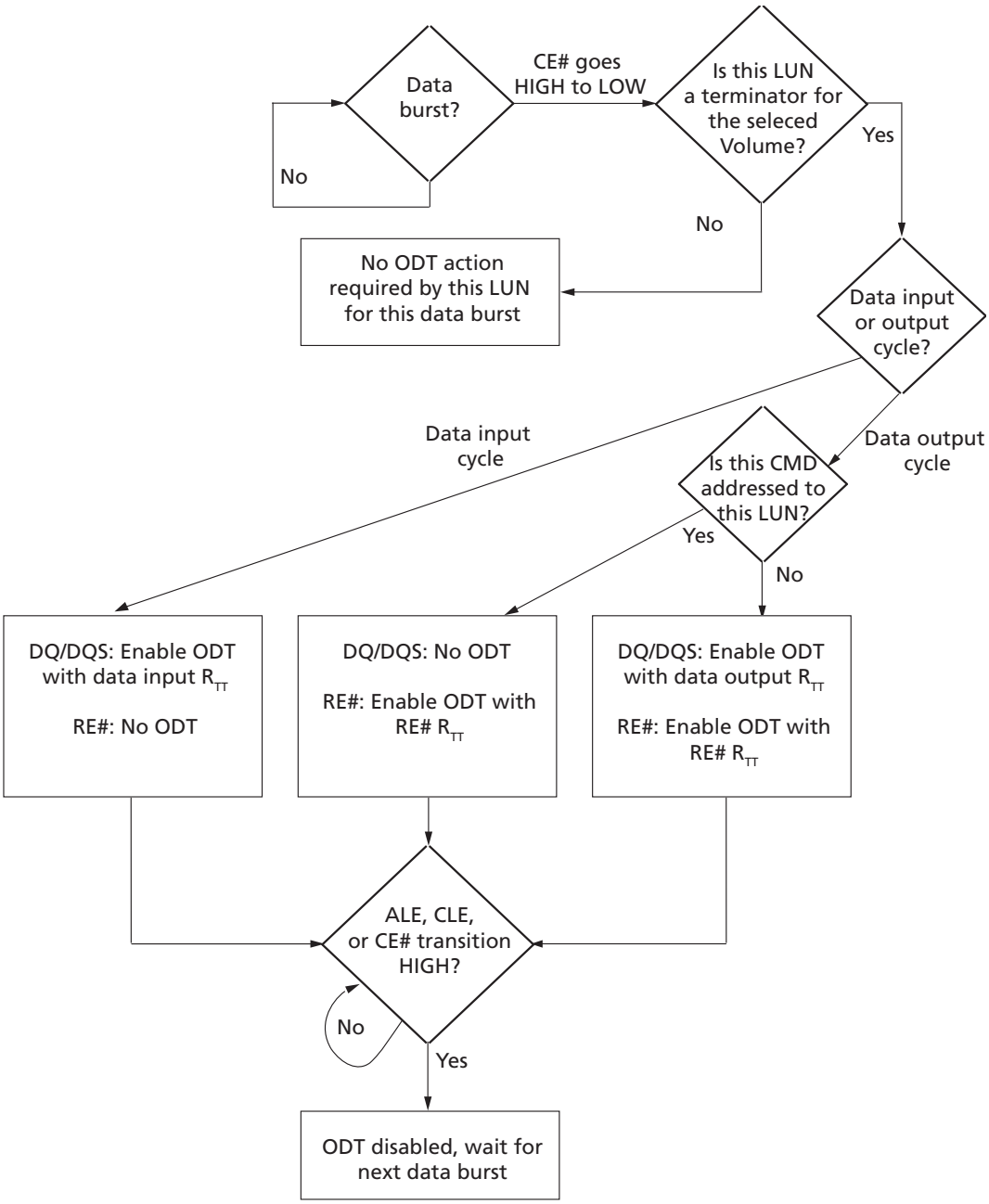
A LUN that is configured to act as a terminator using the configuration matrix (that is specified with the ODT CONFIGURE (E2h) command) may be located on the selected Volume as the Volume it is terminating for (Target termination) or a unselected Volume (non-Target termination). Based on the ODT configuration and the Volume a command is addressed to, LUNs enter different states which determine their ODT behavior; those states are listed in Table 9.

Table 9: LUN state for Matrix Termination

LUN is on selected Volume?	Terminator for selected Volume?	LUN state	ODT actions defined
Yes	N/A	Selected	Figure 21
No	Yes	Sniff	Figure 22
No	No	Deselected	No ODT actions

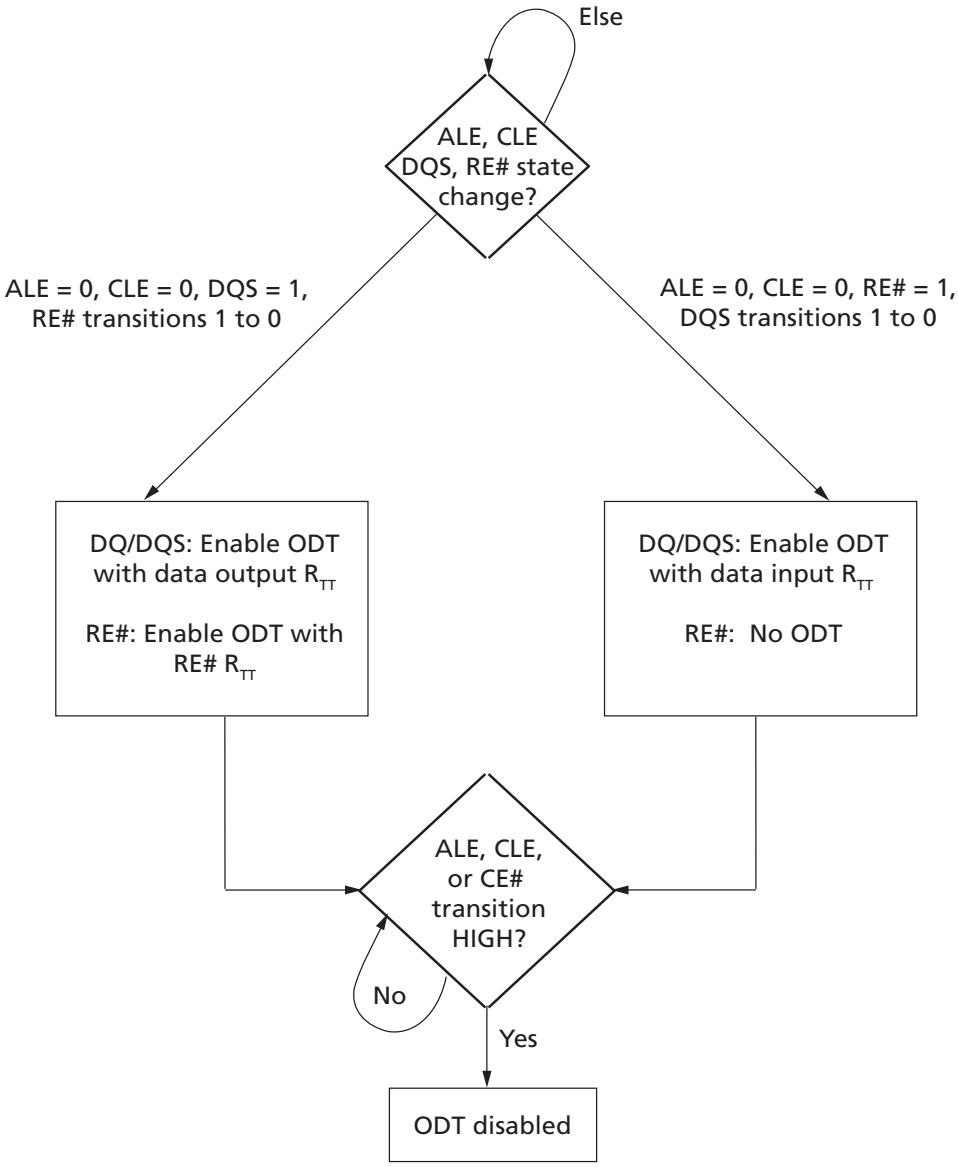
The LUN that a command is addressed to for execution may provide termination. Other LUNs on the selected Volume that are not responsible for execution of the command may also provide termination. Figure 21 defines the ODT actions required for LUNs of each of these types on the selected Volume. LUNs on the selected Volume remain in an active state, and thus are aware of state information like whether there is a data burst currently and the type of cycle; these LUNs do not rely only on ALE, CLE, DQS and RE# signals.

Figure 21: ODT actions for LUNs on selected Volume



The ODT configuration matrix also offers the flexibility of having LUNs on an unselected Volume provide termination for the selected Volume. When a LUN is placed in the Sniff state, it checks the ALE, CLE, DQS and RE# signals to determine when to enable or disable ODT. Figure 22 defines the ODT actions for LUNs in the Sniff state on an unselected Volume.

Figure 22: ODT actions for LUNs in Sniff state on unselected Volume



Matrix Termination Examples

This section describes two examples of on-die termination configurations using matrix termination. In both examples, each Volume consists of two LUNs, referred to as H0N*n*-LUN0 and H0N*n*-LUN1. The following Volume addresses were appointed at initialization.

Table 10: Volume appointment for Matrix Termination example

Volume	Appointed Volume Address
H0N0	0
H0N1	1
H0N2	2
H0N3	3

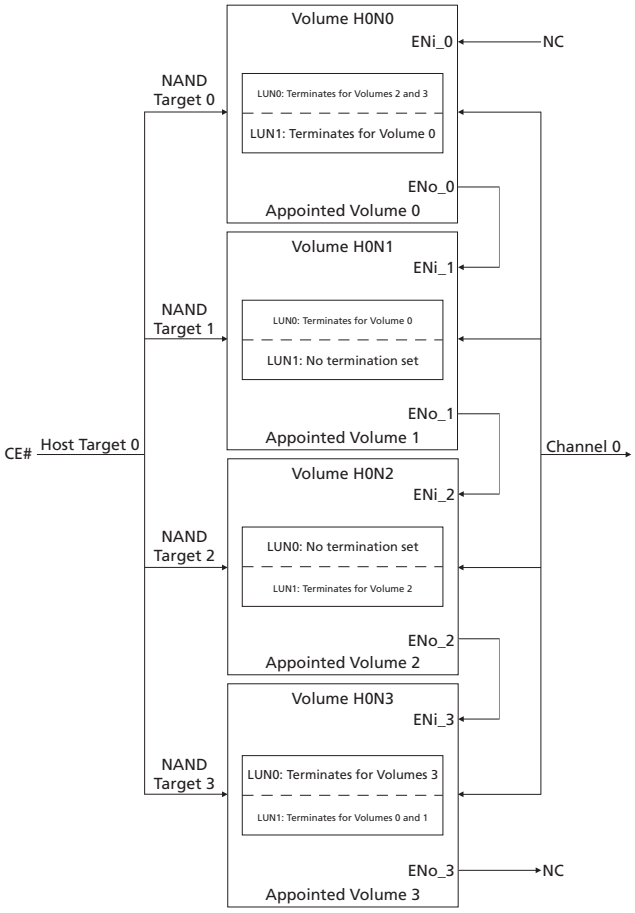
For optimal signal integrity and power consumption, the host may configure termination in a variety of ways. The host may configure a LUN to self terminate, perform non-Target termination for another Volume, or not perform any termination function. Using matrix termination, the termination RTT values may be set differently for each LUN configured as a terminator, including the ability to specify different settings for data output operation and data input operation. The first example shows that a controller may configure the ODT matrix to perform stronger non-Target ODT for data output operations and weaker Target ODT for data input operations.

Table 11: Non-Target ODT for Data Output, Target ODT for Data Input settings configuration example

LUN	Input values for ODT CONFIGURE (E2h)				Notes
	Byte M0	Byte M1	Byte R_{TT1}	Byte R_{TT2}	
H0N0-LUN0	0Ch	00h	40h	00h	Terminates for Volumes 2 and 3 (non-Target) for data output with an R_{TT} value of 50 Ohms for DQ[7:0]/DQS
H0N0-LUN1	01h	00h	02h	03h	Terminates for Volume 0 (Target) for data output with an R_{TT} value of 100 Ohms for DQ[7:0]/DQS and 75 Ohms for RE#
H0N1-LUN0	02h	00h	02h	03h	Terminates for Volume 1 (Target) for data output with an R_{TT} value of 100 Ohms for DQ[7:0]/DQS and 75 Ohms for RE#
H0N1-LUN1	00h	00h	00h	00h	Does not act as a terminator
H0N2-LUN0	00h	00h	00h	00h	Does not act as a terminator
H0N2-LUN1	04h	00h	02h	03h	Terminates for Volume 2 (Target) for data output with an R_{TT} value of 100 Ohms for DQ[7:0]/DQS and 75 Ohms for RE#
H0N3-LUN0	08h	00h	00h	03h	Terminates for Volume 3 (Target) for data output with an R_{TT} value of 100 Ohms for DQ[7:0]/DQS and 75 Ohms for RE#
H0N3-LUN1	03h	00h	40h	00h	Terminates for Volumes 0 and 1 (non-Target) for data output with an R_{TT} value of 50 Ohms for DQ[7:0]/DQS

Note: 1. See ODT CONFIGURE (E2h) for details on input values for ODT CONFIGURE (E2h).

Figure 23: Non-Target ODT for Data Output, Target ODT for Data Input configuration example

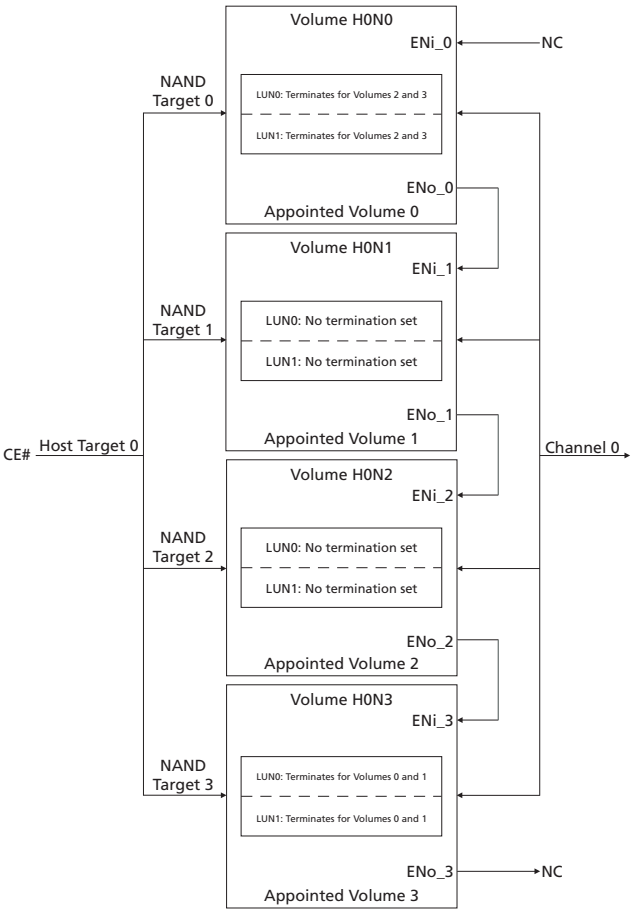


The second example uses parallel non-Target termination to achieve a stronger effective R_{TT} value for both data output and data input operations. For data output, two 50 Ohm terminators are used in parallel to achieve an effective 25 Ohms non-Target termination value. For data input, two 100 Ohm terminators are used in parallel to achieve an effective 50 Ohms non-Target termination value. This type of ODT matrix allows for stronger termination than may be available through a single device. It also allows for intermediate R_{TT} values with the use of different R_{TT} values for parallel LUNs. For example, if one terminator was configured for 75 Ohms and another terminator was configured for 100 Ohms for the same Volume then an effective R_{TT} value of 43 Ohms is achieved. In this example, parallel termination is used for data input and data output for DQ[7:0]/DQS, however, RE# is non-Target terminated with 100 Ohms using a single LUN.

Table 12: Parallel Non-Target ODT settings configuration example

LUN	Input values for ODT CONFIGURE (E2h)				Notes
	Byte M0	Byte M1	Byte R_{TT1}	Byte R_{TT2}	
H0N0-LUN0	0Ch	00h	42h	00h	Terminates for Volumes 2 and 3 (non-Target) for data output with an R_{TT} value of 50 Ohms for DQ[7:0]/DQS. Terminates for Volumes 2 and 3 (non-Target) for data input with an R_{TT} value of 100 Ohms for DQ[7:0]/DQS.
H0N0-LUN1	0Ch	00h	42h	01h	Terminates for Volumes 2 and 3 (non-Target) for data output with an R_{TT} value of 50 Ohms for DQ[7:0]/DQS. Terminates for Volumes 0 and 1 (non-Target) for data input with an R_{TT} value of 100 Ohms for DQ[7:0]/DQS. Terminates for Volumes 2 and 3 (non-Target) with an R_{TT} value of 150 Ohms for RE#.
H0N1-LUN0	00h	00h	00h	00h	Does not act as a terminator
H0N1-LUN1	00h	00h	00h	00h	Does not act as a terminator
H0N2-LUN0	00h	00h	00h	00h	Does not act as a terminator
H0N2-LUN1	00h	00h	00h	00h	Does not act as a terminator
H0N3-LUN0	03h	00h	42h	01h	Terminates for Volumes 0 and 1 (non-Target) for data output with an R_{TT} value of 50 Ohms for DQ[7:0]/DQS. Terminates for Volumes 0 and 1 (non-Target) for data input with an R_{TT} value of 100 Ohms for DQ[7:0]/DQS. Terminates for Volumes 0 and 1 (non-Target) with an R_{TT} value of 150 Ohms for RE#.
H0N3-LUN1	03h	00h	42h	00h	Terminates for Volumes 0 and 1 (non-Target) for data output with an R_{TT} value of 50 Ohms for DQ[7:0]/DQS. Terminates for Volumes 0 and 1 (non-Target) for data input with an R_{TT} value of 100 Ohms for DQ[7:0]/DQS.

Figure 24: Parallel Non-Target ODT configuration example



NV-DDR2 Standby

Prior to disabling a target, the target's bus must be idle. A target is disabled when CE# is driven HIGH, even when it is busy. All of the target's signals are disabled except CE#, WP#, and R/B#.

A target enters low-power standby when it is disabled and is not busy. If the target is busy when it is disabled, the target enters standby after all of the die (LUNs) complete their operations.

NV-DDR2 Idle

A target's bus is idle when CE# is LOW, ALE is LOW, CLE is LOW, RE# is HIGH, and DQS is HIGH and no internal LUN operations are ongoing or data being inputted or outputted from the target. DQS is driven HIGH to prevent the device from enabling ODT. If ODT is disabled, then DQS is a “Don't Care” during Idle states.

During the bus idle mode, all signals are enabled. No commands, addresses, or data are latched into the target; no data is output.

NV-DDR2 Pausing Data Input/Output

Pausing data input or data output may be done by placing the bus in an Idle state. The pausing of data output may also be done by pausing RE# and holding the signal(s) static HIGH or LOW until the data burst is resumed. The pausing of data input may also be done by pausing DQS and holding the signal(s) static HIGH or LOW until the data burst is resumed. WE# shall be held HIGH during data input and output burst pause time. ODT (if enabled) stays ON the entire pause time and warmup cycles (if enabled) are not re-issued when re-starting a data burst from pause. The host will be required to exit the data burst if it wishes to disable ODT or re-issue warmup cycles when re-starting. If the host wishes to end the data burst, after exiting the data burst, a new command is issued.

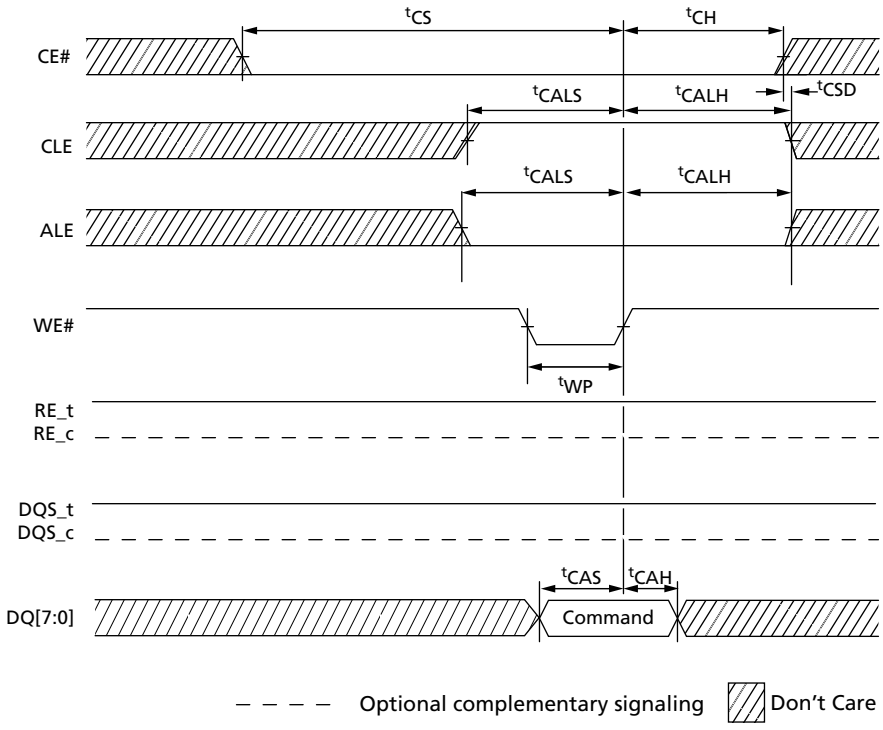
During the bus idle mode, all signals are enabled. No commands, addresses, or data are latched into the target; no data is output.

NV-DDR2 Commands

A command is written from DQ[7:0] to the command register on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is HIGH, and RE# is HIGH.

Commands are typically ignored by die (LUNs) that are busy (RDY = 0); however, some commands, such as READ STATUS (70h) and READ STATUS ENHANCED (78h), are accepted by die (LUNs), even when they are busy.

Figure 25: NV-DDR2 Command Cycle



Note: DQS is "Don't Care" during active command cycle (CLE is high).

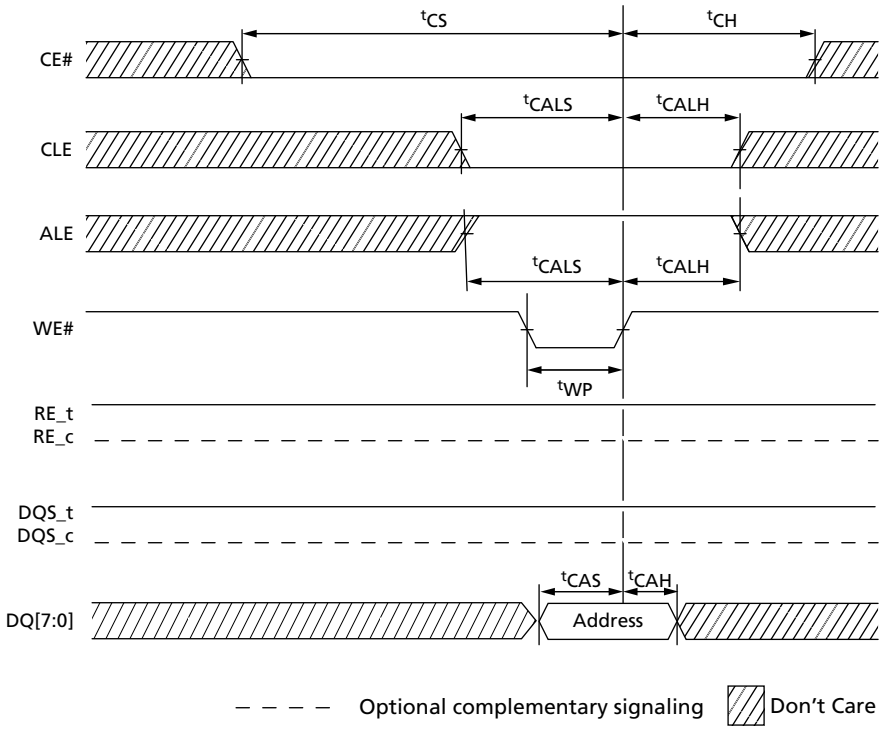
NV-DDR2 Addresses

A NV-DDR2 address is written from DQ[7:0] to the address register on the rising edge of WE# when CE# is LOW, ALE is HIGH, CLE is LOW, and RE# is HIGH.

Bits not part of the address space must be LOW (see Device and Array Organization). The number of address cycles required for each command varies. Refer to the command descriptions to determine addressing requirements.

Addresses are typically ignored by die (LUNs) that are busy (RDY = 0); however, some addresses such as address cycles that follow the READ STATUS ENHANCED (78h) command, are accepted by die (LUNs), even when they are busy.

Figure 26: NV-DDR2 Address Cycle



Note: DQS is "Don't Care" during active address cycle (ALE is high).

NV-DDR2 Data Input

To enter the NV-DDR2 data input mode, the following conditions must be met:

- CE# is LOW
- ALE and CLE are LOW
- RE# is HIGH
- ^{t}WPRE is met
- DQS is LOW

Upon entering the NV-DDR2 data input mode after ^{t}WPRE, data is written from DQ[7:0] to the cache register on each and every rising and falling edge of DQS (center-aligned) when CE# is LOW, RE# is HIGH, and ALE and CLE are LOW.

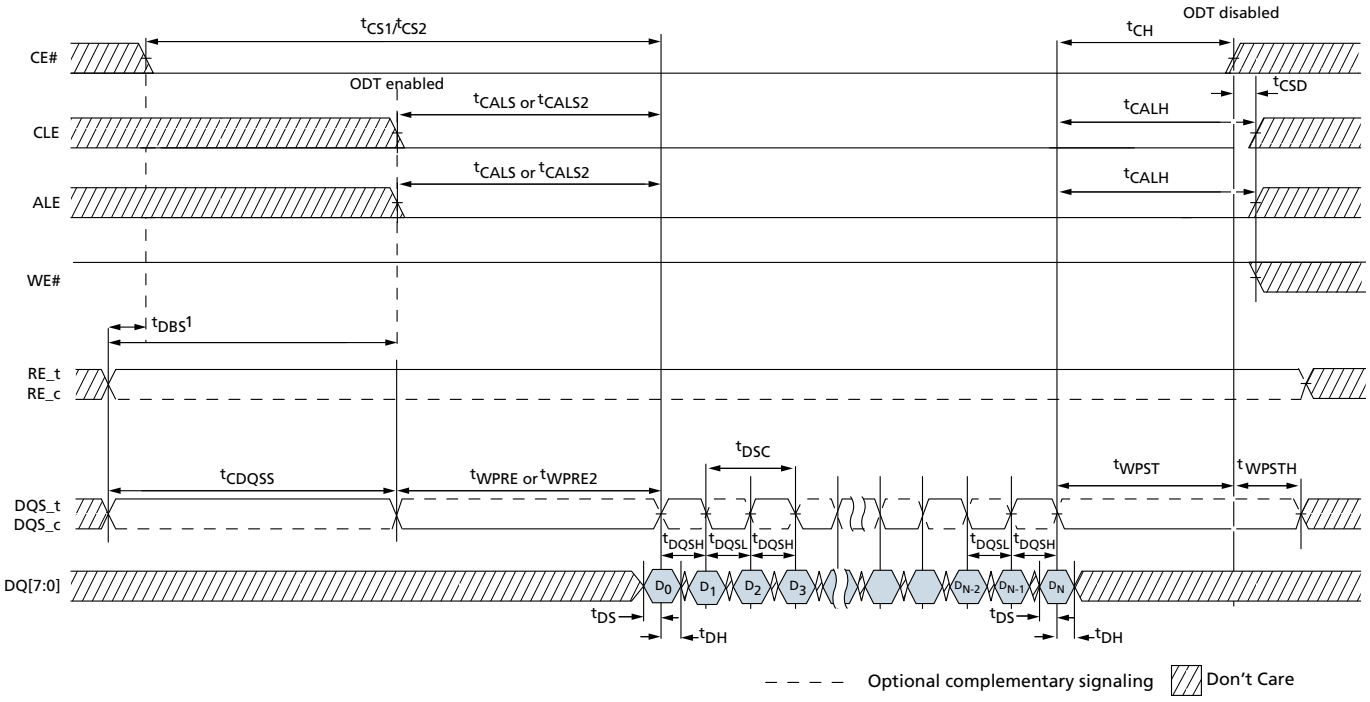
To exit NV-DDR2 data input mode, the following conditions must be met:

- CE# is LOW
- ALE and CLE are LOW
- RE# is HIGH
- The final two data bytes of the data input sequence are written to DQ[7:0] to the cache register on the rising and falling edges of DQS after the last cycle in the data input sequence
- DQS is held LOW for ^{t}WPST (after the final falling edge of DQS)

Following ^{t}WPST, the bus enters bus idle mode.

Data input is ignored by die (LUNs) that are not selected or are busy.

Figure 27: NV-DDR2 Data Input Cycles



Notes: 1. ODT may not be required to be used for data input. If ODT is selected for use via SET FEATURES (EFh), then ODT is enabled and disabled during the points indicated.

NV-DDR2 Data Output

Data can be output from a die (LUN) if it is ready. Data output is supported following a READ operation from the NAND Flash array.

To enter the NV-DDR2 data output mode, the following conditions must be met:

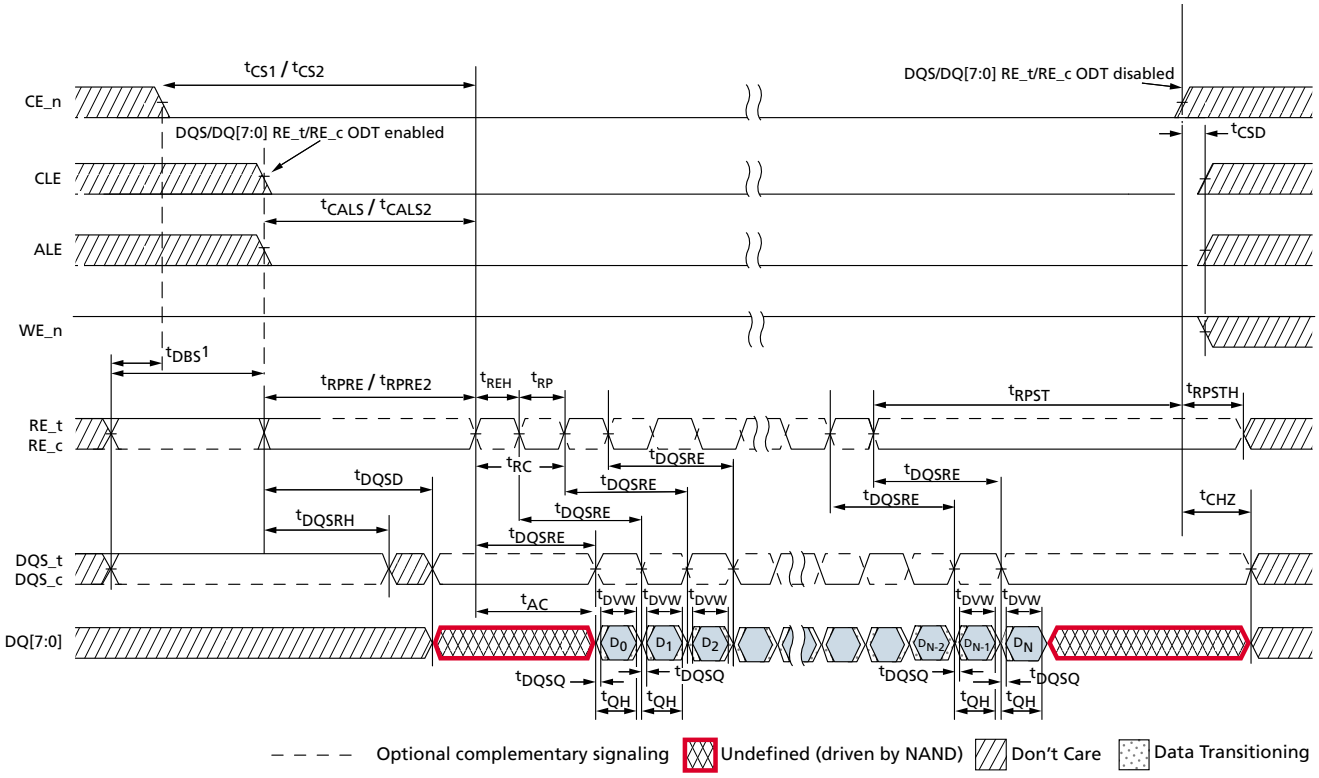
- CE# is LOW
- The host has released the DQ[7:0] bus and DQS
- ALE and CLE are LOW
- ^{t}RPRE is met

Upon entering the NV-DDR2 data output mode, DQS will toggle HIGH and LOW with a delay of ^{t}DQSRE from the respective rising and falling edges of RE#. DQ[7:0] will output data edge-aligned to the rising and falling edges of DQS, with the first transition delayed by no more than ^{t}AC.

The final two data bytes are output on DQ[7:0] on the final rising and falling edges of DQS. The final rising and falling edges of DQS occur ^{t}DQSRE after the last cycle in the data output sequence. The host must hold RE# for ^{t}RPST after the last RE# falling edge for data output.

Data output requests are typically ignored by a die (LUN) that is busy (RDY = 0); however, it is possible to output data from the status register even when a die (LUN) is busy by issuing the READ STATUS (70h) or READ STATUS ENHANCED (78h) command.

Figure 28: NV-DDR2 Data Output Cycles



Notes: 1. ODT may not be required to be used for data output. If ODT is selected for use via SET FEATURES (EFh), then ODT is enabled and disabled during the points indicated.
2. ^{t}DQSRH is only required if matrix ODT is enabled.

Write Protect

See Write Protect under Bus Operation – Asynchronous Interface.

Ready/Busy#

See Ready Busy under Bus Operation – Asynchronous Interface.

V_{CC} Power Cycling

Some NAND Flash devices do not support V_{CCQ}. For these devices all references to V_{CCQ} are replaced with V_{CC}.

SpecTek NAND Flash devices are designed to prevent data corruption during power transitions. V_{CC} is internally monitored. (The WP# signal supports additional hardware protection during power transitions. When ramping V_{CC} and V_{CCQ}, use the following procedure to initialize the device:

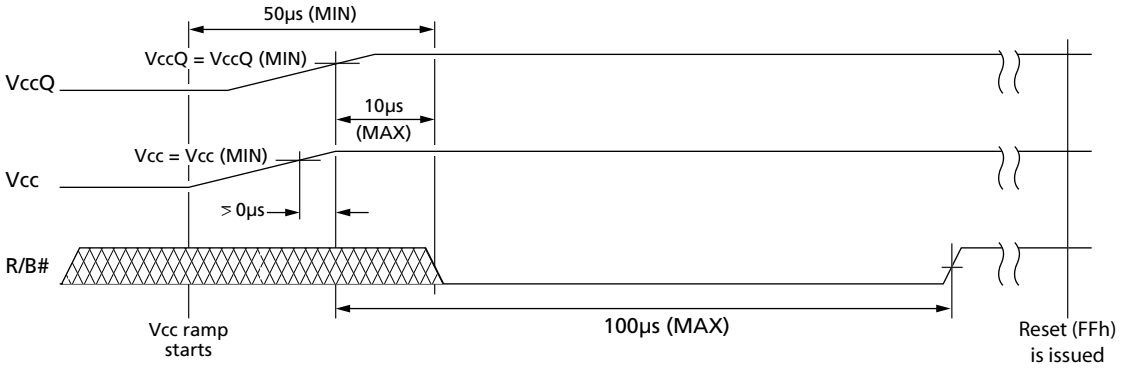
1. Ramp V_{CC}.
2. Ramp V_{CCQ} and V_{CCQ} must not exceed V_{CC}.
3. The host must wait for R/B# to be valid and HIGH before issuing RESET (FFh) to any target (see Figure 29). The R/B# signal becomes valid when 50µs has elapsed since the beginning the VCC ramp, and 10µs has elapsed since V_{CCQ} reaches V_{CCQ} (MIN) and V_{CC} reaches V_{CC} (MIN).
4. If not monitoring R/B#, the host must wait at least 100µs after V_{CCQ} reaches V_{CCQ} (MIN) and V_{CC} reaches V_{CC} (MIN). If monitoring R/B#, the host must wait until R/B# is HIGH.
5. If V_{CCQ} is in the 1.8V operational range, then the asynchronous interface is active by default for each target. Each LUN draws less than an average of I_{ST} measured over intervals of 1ms until the RESET (FFh) command is issued.
6. The RESET (FFh) command must be the first command issued to all targets (CE#s) after the NAND Flash device is powered on. Each target will be busy for ^{t}POR after a RESET command is issued. LUN0 of each target is selected by default after power-on. The RESET busy time can be monitored by polling R/B# or by using the READ STATUS (70h) command. For multi-LUN configurations the READ STATUS ENHANCED (78h) command should be used to check initialization status of each LUN on the target. The host must not issue an additional RESET (FFh) command during ^{t}POR.
7. The device is now initialized and ready for normal operation.

At power-down, V_{CCQ} must go LOW, either before, or simultaneously with, V_{CC} going LOW.

When V_{CCQ} = 0V, the host must keep RE_t/RE_c, DQS_t/DQS_c signals LOW. RE_t/RE_c, DQS_t/DQS_c signals maybe ramped with V_{CCQ} during power up but not exceed V_{CCQ}. When V_{CCQ} = 0V, the host must keep DQ[7:0] signals LOW or they can be left High-Z. DQ[7:0] signals may be ramped with V_{CCQ} during power up but not exceed V_{CCQ}.

It is not permitted to drive or have the NAND R/B# signal HIGH while the NAND V_{CCQ} voltage is below $V_{CCQ,min}$. R/B# signals maybe ramped with V_{CCQ} during power up but not exceed V_{CCQ}.

Figure 29: R/B# Power-On Behavior



Notes: 1. Disregard V_{CCQ} for devices that use only V_{CC}.

To initialize a discovered target, the following steps shall be taken. The initialization process should be followed for each connected CE# signal, including performing the READ PARAMETER PAGE (ECh) command for each target. Each chip enable corresponds to a unique target with its own independent properties that the host shall observe and subsequently use.

The host should issue the READ PARAMETER PAGE (ECh) command. This command returns information that includes the capabilities, features, and operating parameters of the device. When the information is read from the device, the host shall check the CRC to ensure that the data was received correctly and without error prior to taking action on that data.

If the CRC of the first parameter page read is not valid, the host should read redundant parameter page copies. The host can determine whether a redundant parameter page is present or not by checking if the first four bytes contain at least two bytes of the parameter page signature. If the parameter page signature is present, then the host should read the entirety of that redundant parameter page. The host should then check the CRC of that redundant parameter page. If the CRC is correct, the host may take action based on the contents of that redundant parameter page. If the CRC is incorrect, then the host should attempt to read the next redundant parameter page by the same procedure.

The host should continue reading redundant parameter pages until the host is able to accurately reconstruct the parameter page contents. The host may use bit-wise majority or other ECC techniques to recover the contents of the parameter page from the parameter page copies present. When the host determines that a parameter page signature is not present, then all parameter pages have been read.

After successfully retrieving the parameter page, the host has all information necessary to successfully communicate with that target. If the host has not previously mapped defective block information for this target, the host should next map out all defective blocks in the target. The host may then proceed to utilize the target, including erase and program operations.

Electronic Mirroring

Electronically mirrored DQ[7:0] pinout is available in order to assist in optimizing printed circuit board (PCB) layout by assisting two-sided (clamshell) designs in reducing the complexity and the number of signal routing layers between the top and bottom side of the PCB. This ability for electronic mirrored DQ[7:0] pinout also assists in reducing the vertical profile of a two-sided system. Only the DQ[7:0] signals have the ability to be changed by electronic mirrored functionality, all other NAND signals remain static.

See Figure 30 and Figure 31 as examples of how packages in the default non-mirrored DQ[7:0] pinout and the mirrored DQ[7:0] pinout could be used in a two-sided PCB system.

Figure 30: Example PCB Layout of a Two-Sided System without Electronic Mirroring of DQ[7:0]

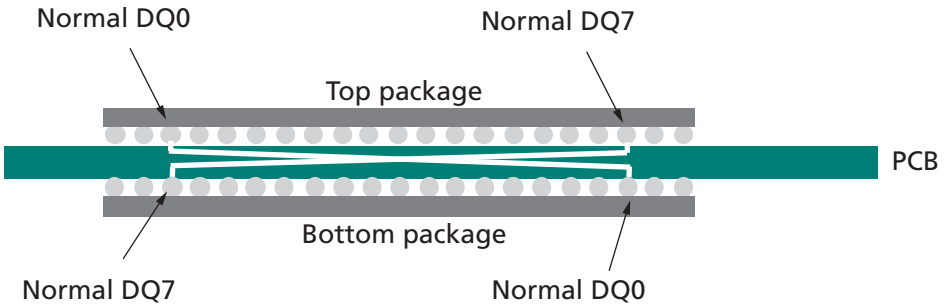
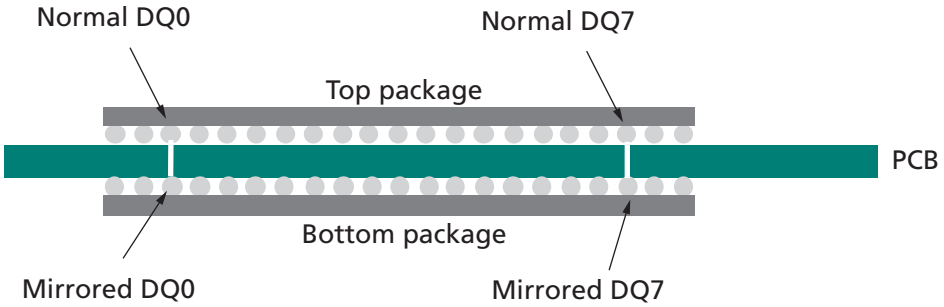


Figure 31: Example PCB Layout of a Two-Sided System with Electronic Mirroring of DQ[7:0]



The mirror and non-mirrored packages are physically the same with same internal bond connections, but based on how first issued command after device initialization is decoded, the LUNs internally are electrically configured to be non-mirrored or mirrored.

If using the mirrored DQ[7:0] pinout configuration, the READ STATUS (70h) command must be issued in order to properly configure the device DQ[7:0] signals as mirrored or non-mirrored mode after device initialization. This READ STATUS (70h) command appears as “0Eh” on the DQ[7:0] bus of the NAND device in the mirrored position; “0Eh” is not a valid command and is recognized by the NAND device as a 70h command which is the indication to the NAND target (CE#) to configure itself into mirrored DQ[7:0]

mode. The READ STATUS (70h) command needs be issued only once per target (CE#) or volume after device initialization for a device in the mirrored position; the device in the mirrored position will remain in the mirrored DQ[7:0] mode until device power-down.

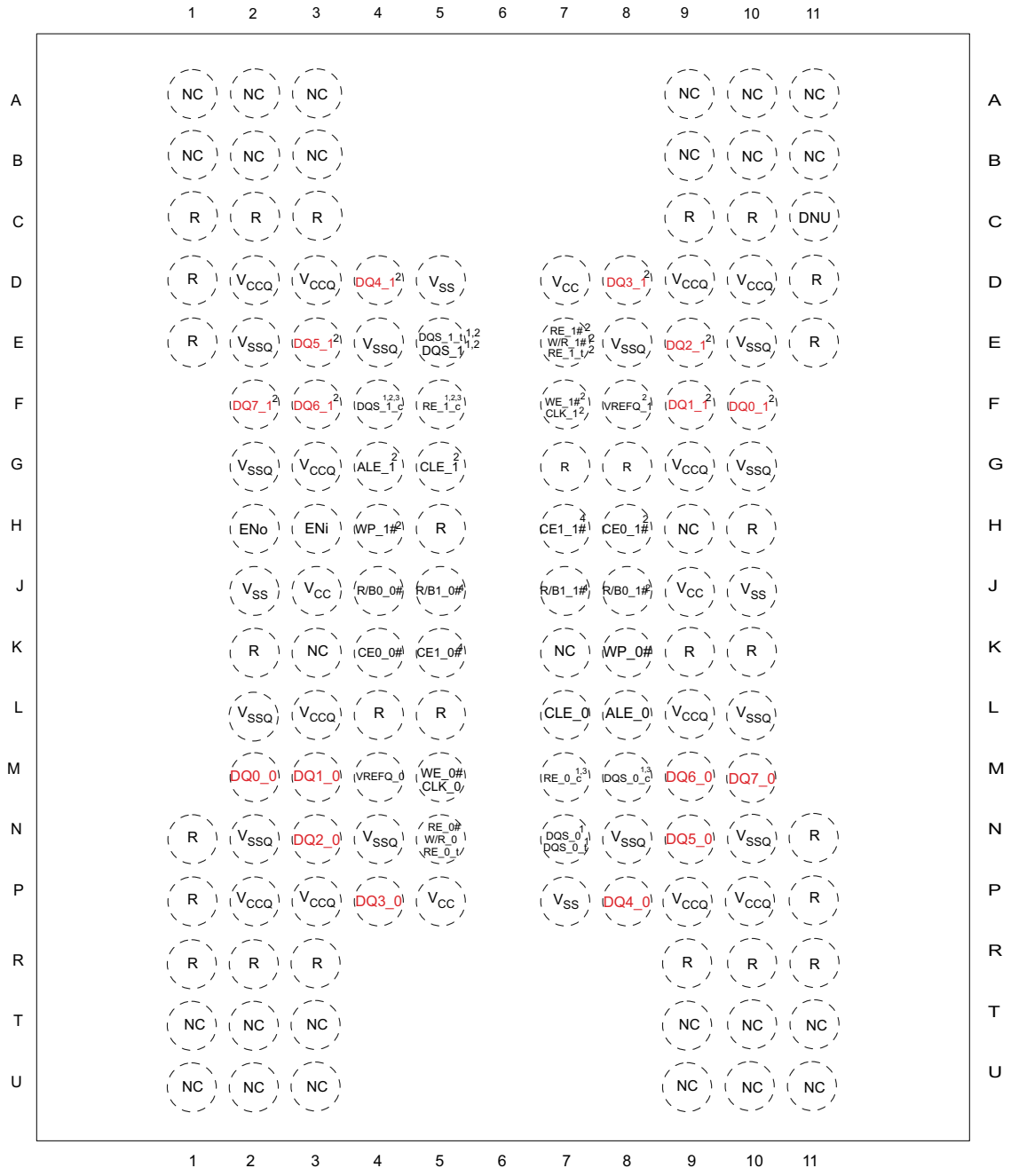
If the READ STATUS (70h) command is issued prior to first RESET (FFh) and CE# pin reduction is enabled, then sequential initialization is enabled. If the READ STATUS (70h) command is issued after the first RESET (FFh) and CE# pin reduction is enabled, then parallel initialization is enabled.

Only the 132-ball and/or 152-ball BGA packages offer electronic mirroring operations. The 272-ball BGA package will not support electronic mirroring due to the limitation of DQ[7:0] signal assignment ordering.

See Figure 32 as an example of how a package in the mirrored DQ[7:0] pinout changes signal assignments for the DQ[7:0] signals.

A HARD RESET (FDh) command will not change a device from the mirrored pinout configuration to the non-mirrored pinout configuration.

Figure 32: Example of 132-Ball BGA Package in Mirrored DQ[7:0] Pinout



Note: Note the DQ[7:0] signals highlighted in red for the mirrored pinout configuration in comparison to the default non-mirrored pinout configuration. See the Signal Assignments section for the default non-mirrored pinout configuration for this package.

Activating Interfaces

After performing the steps under Bus Operation – NV-DDR2 Interface, the asynchronous interface is active for all targets on the device when the device powers on within the 1.8V V_{CCQ} operational range.

Each target's interface is independent of other targets, so the host is responsible for changing the interface for each target.

If the host and NAND Flash device, through error, are no longer using the same interface when within the 1.8V V_{CCQ} operational range, then steps under Activating the Asynchronous Interface are performed to re-synchronize the interfaces.

Activating the Asynchronous Interface

To activate the asynchronous NAND interface, the following steps are repeated for each target:

1. The host pulls CE# HIGH, disables its input to CLK, and enables its asynchronous interface.
2. The host pulls CE# LOW and issues the RESET (FFh) command, using an asynchronous command cycle.
3. R/B# goes LOW for ^{t}RST.
4. After ^{t}ITC, and during ^{t}RST, the device enters the asynchronous NAND interface. READ STATUS (70h) and READ STATUS ENHANCED (78h) are the only commands that can be issued.
5. After ^{t}RST, R/B# goes HIGH. TIMING MODE feature address (01h), sub-feature parameter P1 is set to 00h, indicating that the asynchronous NAND interface is active and that the device is set to timing mode 0.

For further details, see Reset Operations.

Activating the NV-DDR Interface

To activate the NV-DDR NAND Flash interface, the following steps are repeated for each target:

1. Issue the SET FEATURES (EFh) command.
2. Write address 01h, which selects the TIMING MODE feature address.
3. Write P1 with 1Xh, where “X” is the timing mode used in the NV-DDR interface (see Configuration Operations).
4. Write P2–P4 as 00h-00h-00h.
5. R/B# goes LOW for ^{t}ITC. The host should pull CE# HIGH. During ^{t}ITC, the host should not issue any type of command, including status commands, to the NAND Flash device.
6. After ^{t}ITC, R/B# goes HIGH and the synchronous interface is enabled. Before pulling CE# LOW, the host should enable the clock.

Activating the NV-DDR2 Interface

Transitions from NV-DDR directly to NV-DDR2 (or vice versa) is not supported. In this case, the host should transition to the asynchronous interface and then select the desired synchronous interface.

Prior to selecting the NV-DDR2 interface, it is recommended that settings for the NVDDR2 interface be configured. Specifically:

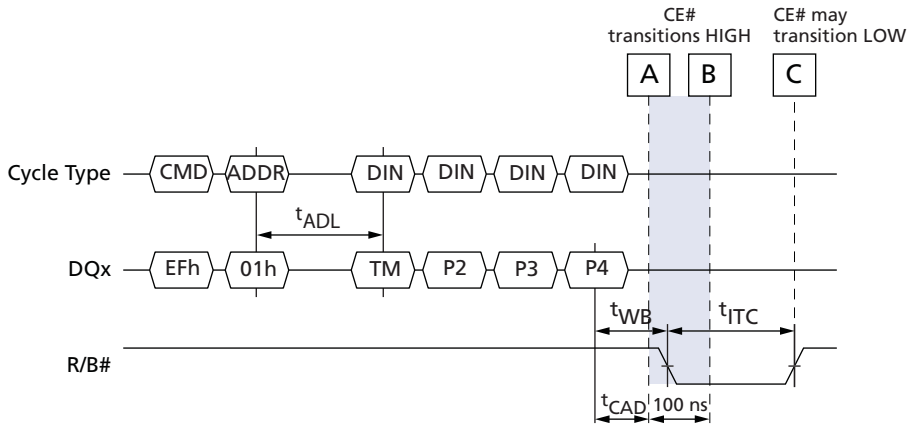
- SET FEATURES (EFh) command should be used to configure the NV-DDR2 Configuration feature address.

These actions should be completed prior to selecting the NV-DDR2 interface. If these settings are modified when the NV-DDR2 interface is already selected, the host should take care to ensure appropriate settings are applied in a manner that avoids signal integrity issues.

To activate the NV-DDR2 NAND Flash interface, the following steps are repeated for each target:

1. Issue the SET FEATURES (EFh) command.
2. Write address 01h, which selects the Timing mode feature address.
3. Write P1 with 2Xh, where "X" is the timing mode used in the NV-DDR2 interface (see Configuration Operations)
4. Write P2–P4 as 00h-00h-00h.
5. R/B# goes LOW for ^{t}ITC. The host should pull CE# HIGH. During ^{t}ITC, the host should not issue any type of command, including status commands, to the NAND Flash device.
6. After ^{t}ITC, R/B# goes HIGH and the NV-DDR2 interface is enabled.

Figure 33: Activating Interfaces



Notes: 1. TM = Timing Mode

CE# Pin Reduction and Volume Addressing

In higher density capacity implementations there may be a significant number of CE# pins required for a host to support where there are many NAND packages with two to four CE# pins per package. The CE# pin reduction mechanism enables a single CE# pin from the host to be shared by multiple NAND targets, thus enabling a significant reduction in the number of CE# pins required by the host system. The CE# pin reduction mechanism may be utilized with any data interface (asynchronous, NV-DDR, NV-DDR2).

In the CE# pin reduction mechanism, each NAND package is appointed a volume address during the initialization sequence. After initialization is complete, the host may address a particular volume (NAND target) by using the VOLUME SELECT (E1h) command. See VOLUME SELECT (E1h) for more details.

ENi and ENo pins are added to each NAND package and a daisy chain is created between NAND packages. The first NAND package in the chain has the ENi pin as not connected. All other NAND packages have their ENi pin connected to the previous package's ENo pin in a daisy chain configuration.

At power-on, the ENo pins are driven LOW by the NAND device. ENo shall be High-Z when all CE# signals on the NAND package are HIGH. When a NAND target has had a volume address appointed with the SET FEATURES (EFh) command, then the ENo pin shall be pulled HIGH by the NAND target when the corresponding CE# is LOW. This enables the next NAND target on a subsequent package in the daisy chain to accept commands because the ENi pin pulls HIGH when ENo is no longer pulling LOW. After a volume address has been appointed to a volume (for example, NAND target), that volume shall become deselected and ignores the ENi pin until the next power cycle.

The state of ENi determines whether the NAND package is able to accept commands. If the ENi pin is HIGH and CE# is LOW for the NAND target, then the NAND target shall accept commands. If the ENi pin is LOW or CE# is HIGH for the NAND target, then the NAND target shall not accept commands.

To be selected to process a command, the VOLUME SELECT command shall be issued to the host target using the volume address that was previously appointed for a particular NAND target. After the CE# signal is pulled HIGH for ^{t}CEH time, all LUNs on a volume revert to their previous states.

A HARD RESET (FDh) command will not undo CE# Pin Reduction or any previously set volume addressing assignments that were performed prior to the HARD RESET (FDh) command.

Figure 34: CE# Pin Reduction Topology with single channel

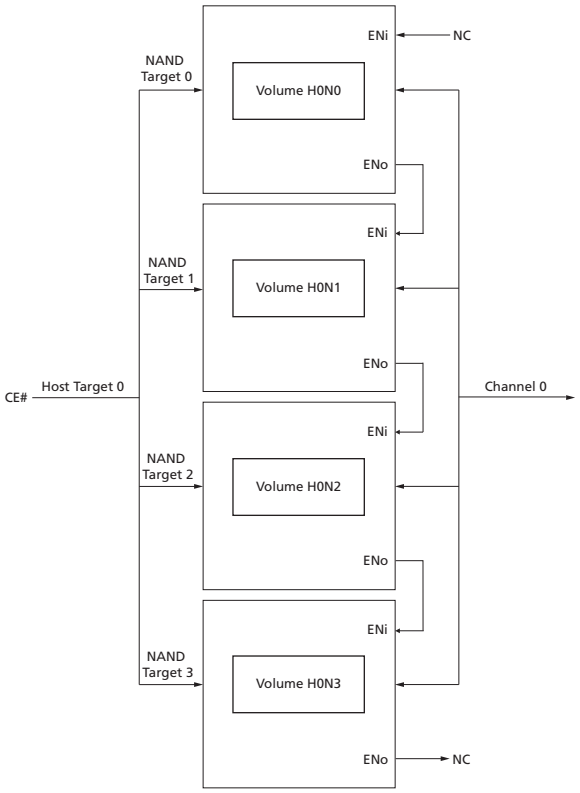
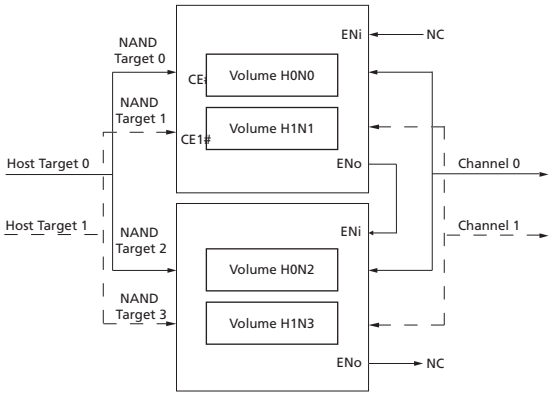


Figure 35: CE# Pin Reduction and Volume Addressing Topology with dual channel



Initialization Sequence

The host may issue a RESET (FFh) to all Targets in parallel on the selected Host Target, or the host may sequentially issue RESET (FFh) to each Target. The methodology chosen depends on host requirements for maximum current draw. To reset all Targets in parallel, the host issues a RESET (FFh) as the first command issued to the NAND device(s). To reset Targets sequentially, the host issues a READ STATUS (70h) command as the first command issued to all NAND Targets on the selected Host Target.

During initialization when addressing a newly selected NAND Target with an initial command, the host shall wait for the ENo signal to be propagated to the ENi of the subsequent Target. Before addressing a new Target, the host shall wait (^{t}ENo + ^{t}ENi) and should also include signal propagation time.

In cases where there are multiple NAND targets within a package (multiple CE#), those NAND targets share the same ENo signal, and the host shall not stagger SET FEATURES (EFh) commands that appoint the volume addresses. If the SET FEATURES (EFh) commands are not issued simultaneously, then the host shall wait until volume appointment for previous NAND target(s) is complete before issuing the next SET FEATURES (EFh) command to appoint the volume address for the next NAND target that shares the ENo within a package.

After issuing the SET FEATURE (EFh) command to appoint the Volume address, the host shall not issue another command to any NAND Target on the associated Host Target (including status commands) until after the ^{t}FEAT time has elapsed. This is to ensure that the proper NAND Target responds to the next command, allowing for the proper ENo/ENi signal levels to be reflected.

The initialization sequence when utilizing the CE# reduction functionality is as follows:

1. The host powers on the NAND device(s).
2. The host pulls CE# LOW.
3. If resetting all NAND Targets in parallel, then the host issues the RESET (FFh) command. This command is accepted by all NAND Targets connected to the CE# (Host Target).
4. If resetting each NAND Target sequentially, then:
   a. The host issues the READ STATUS (70h) command to check for ready status. Issuing the READ STATUS (70h) command prior to any other command indicates sequential RESET (FFh) of each NAND target. The host then issues the RESET (FFh) command, which is only accepted by NAND devices with ENi set HIGH.
5. The host issues a READ STATUS (70h) command and waits for the device to be ready (RDY = 1; ARDY = 1).
6. The host configures the NAND Target via commands necessary to perform that function (READ PARAMETER PAGE (ECh) command, SET FEATURES (EFh) command, and so forth).
7. The host issues SET FEATURES (EFh) command to the Volume Configuration feature address to appoint the Volume address for the NAND Target. The Volume Address specified shall be unique amongst all NAND Targets. After the SET FEATURE (EFh) command completes, ENo is set to one and the Volume is deselected until a VOLUME SELECT (E1h) command is issued that selects the Volume. The host shall not issue another command to a NAND Target connected to the associated Host Target until after ^{t}FEAT time has elapsed.
8. For each NAND target connected to a host target, steps 4–7 are repeated for sequential initialization, and steps 5–7 are repeated for parallel initialization.
9. When no further NAND targets are found connected to the host target, then repeat steps 2–8 for the next host target (for example, host CE# pin).

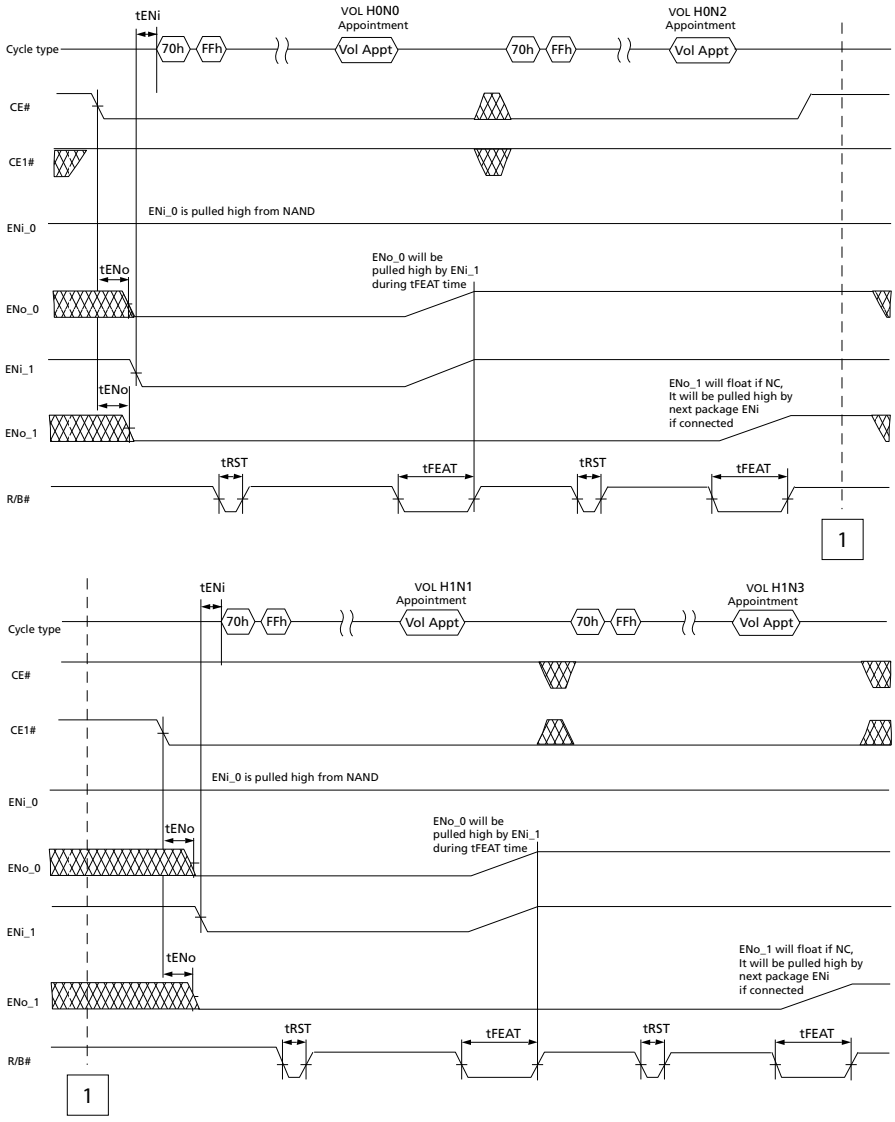
10. To complete the initialization process, a VOLUME SELECT (E1h) command is issued to select the next Volume that is going to execute a command.

After volume addresses have been appointed to all NAND targets, the host may complete any additional initialization tasks (for example, configure on-die termination (ODT) for the NV-DDR2 interface) and then proceed with normal operation. Prior to issuing a command to a volume, the VOLUME SELECT (E1h) command shall be issued.

The host CE# signal shall be kept LOW for steps 2–7. If the host CE# signal that is LOW for steps 2–7 is brought HIGH anytime after step 7 but before the initialization process is complete, then ^{t}CS for asynchronous timing mode 0 shall be used.

Figure 36 is an example of sequential reset initialization for the CE# pin reduction topology of Figure 35.

Figure 36: Example of Sequential Reset Initialization



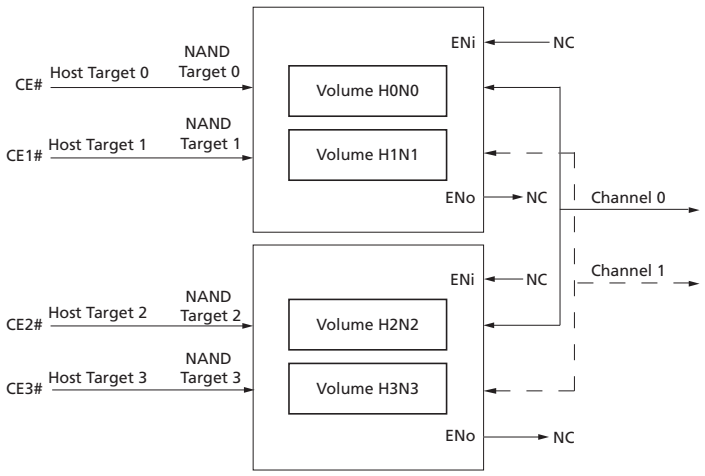
Volume Appointment without CE# Pin Reduction

If CE# pin reduction is not used (for example, if ENi and ENo are not connected) and the host desires to have the terminator on a package that does not share a CE# with the selected NAND target, then each package that shares the CE# must have a volume appointed at initialization using the SET FEATURE (EFh) command using the volume configuration feature.

Each CE# must have a unique volume address appointed. Once all NAND targets have volume addresses appointed, the appointed volume addresses may be used for termination selection. Volume addressing is not required for operation due to discrete CE# signals; however, the VOLUME SELECT (E1h) command is required for terminator selection when using non-target termination schemes.

During operation, the CE# signal for the selected volume and for any NAND targets assigned as a terminator for the selected volume need to be brought LOW. When CE# is brought LOW for an unselected volume, all LUNs that are not assigned as terminators for the selected volume are deselected.

Figure 37: Volume Addressing without CE# Pin Reduction Topology with Dual Channel



Appointing Volume Addresses

To appoint a volume address, the SET FEATURE command is issued with a feature address of volume configuration. The volume address is not retained across power cycles; thus, if volume addressing is going to be used it needs to be appointed after each power-on prior to use of the NAND device(s). The volume address is retained when HARD RESET (FDh) command is issued.

Selecting a Volume

After volume addresses have been appointed, every NAND target (and associated LUN) is selected when the associated CE# is pulled LOW. After CE# is held LOW for at least 100ns, the host issues a VOLUME SELECT (E1h) command to indicate the volume (NAND target) that shall execute the next command issued.

Multiple Volume Operation Restriction

Volumes are independent entities. A multiple volume operation is when two or more volumes are simultaneously processing commands. Before issuing a command to an unselected Volume, CE# shall be pulled HIGH for a minimum of ^{t}CEH and the VOLUME SELECT (E1h) command shall then be issued to select the volume to issue a command to next. While commands (including multi-LUN operations) are being performed on the selected Volume, a VOLUME SELECT (E1h) command is not required.

Issuing the same command to multiple Volumes at the same time is not supported.

For a LUN level command (for example, READ, PROGRAM), the host may select a different volume during a data input or data output operation and then resume the data transfer operation at a later time for a LUN level command. When re-selecting a volume and associated LUN to complete the data input or data output operation, the following actions are required:

- Data input: The host shall wait ^{t}CCS and then issue a CHANGE ROW ADDRESS (85h) command prior to resuming data input.
- Data output: The host shall issue a CHANGE READ COLUMN ENHANCED (06h-E0h) or RANDOM DATA OUT (00h-05h-E0h) command prior to resuming data output.

For a target level command (GET FEATURES (EEh), SET FEATURES (EFh)), the host shall complete all data input or data output operations associated with that command prior to selecting a new volume.

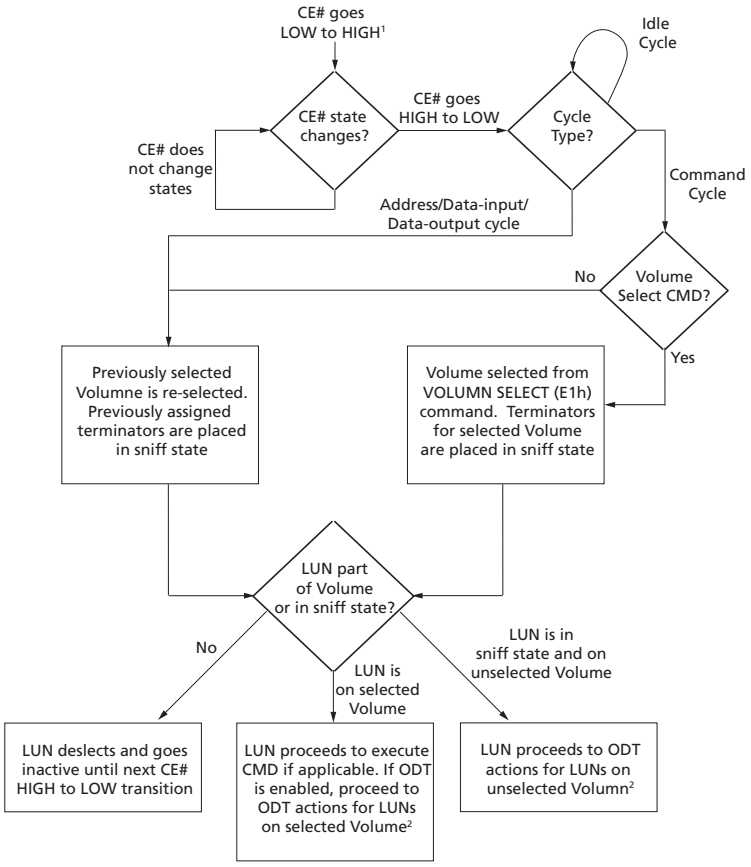
A VOLUME SELECT command shall not be issued during the following atomic portions of the COPYBACK, READ, PROGRAM, and ERASE operations:

- READ operations:
  - READ PAGE (00h-30h)
  - COPYBACK READ (00h-35h)
  - READ PAGE MULTI-PLANE (00h-32h)
- PROGRAM operations, note: The VOLUME SELECT (E1h) command may be issued prior to the 10h, 11h, or 15h command if the next command to this volume is CHANGE ROW ADDRESS (85h). After VOLUME SELECT command is issued to resume data input, the host shall wait ^{t}CCS before issuing CHANGE ROW ADDRESS command:
  - PROGRAM PAGE (80h-10h)
  - PROGRAM PAGE MULTI-PLANE (80h/81h-11h)
  - PROGRAM PAGE CACHE (80h-15h)
  - COPYBACK PROGRAM (85h-10h)
  - COPYBACK PROGRAM MULTI-PLANE (85h-11h)
- ERASE operations:
  - ERASE BLOCK (60h-D0h)
  - ERASE BLOCK MULTI-PLANE (60h-D1h or 60h-60h-D0h)

Volume Reversion

When using volume addressing, the LUNs shall support volume reversion. Specifically, if CE# is transitioned from HIGH to LOW and a volume select is not the first command, then the LUN shall revert to the previously selected, sniff, and deselected states based on the last specified volume address. If on-die termination (ODT) is enabled when using the NV-DDR2 data interface there are additional actions described within on-die termination.

Figure 38: Volume Reversion behavioral flow



Notes: 1. This state is entered asynchronously when CE# transitions from LOW to HIGH.
2. ODT actions for LUNs on a selected Volume are specified in Figure 21. ODT actions for LUNs on an unselected Volume are specified in Figure 22.

Command Definitions

Table 13: Command Set

Command	Command Cycle #1	# Valid Address Cycles	Data Input Cycles	Command Cycle #2	# Valid Address Cycles #2	Command Cycle #3	Valid while Selected LUN is Busy[1]	Valid while Other LUNs are Busy[2]	Notes
RESET Operations									
RESET	FFh	0	—	—	—	—	Yes	Yes	
HARD RESET	FDh	0	—	—	—	—		Yes	
SYNCHRONOUS RESET	FCh	0	—	—	—	—	Yes	Yes	
RESET LUN	FAh	3	—	—	—	—	Yes	Yes	
Identification Operations									
READ ID	90h	1	—	—	—	—			3
READ PARAMETER PAGE	ECh	1	—	—	—	—			
READ UNIQUE ID	EDh	1	—	—	—	—			
Configuration Operations									
VOLUME SELECT	E1h	1	—	—	—	—			
ODT CONFIGURE	E2h	1	4	—	—	—			
GET FEATURES	EEh	1	—	—	—	—			3
SET FEATURES	EFh	1	4	—	—	—			4
GET FEATURES by LUN	D4h	2	—	—	—	—		Yes	3
SET FEATURES by LUN	D5h	2	4	—	—	—		Yes	4
SLC MODE ENABLE	DAh	0	—	—	—	—		Yes	
SLC MODE DISABLE	DFh	0	—	—	—	—		Yes	
STATUS Operations									
READ STATUS	70h	0	—	—	—	—	Yes		
FIXED ADDRESS READ STATUS ENHANCED	71h	1	—	—	—	—	Yes	Yes	
SELECT LUN WITH STATUS	78h	3	—	—	—	—	Yes	Yes	
Column Address Operations									
CHANGE READ COLUMN	05h	2	—	E0h	—	—		Yes	
CHANGE READ COLUMN ENHANCED (ONFI)	06h	5	—	E0h	—	—		Yes	
CHANGE READ COLUMN ENHANCED (JEDEC)	00h	5	—	05h	2	E0h		Yes	
CHANGE WRITE COLUMN	85h	2	Optional	—	—	—		Yes	

Table 13: Command Set (Continued)

Command	Command Cycle #1	# Valid Address Cycles	Data Input Cycles	Command Cycle #2	# Valid Address Cycles #2	Command Cycle #3	Valid while Selected LUN is Busy[1]	Valid while Other LUNs are Busy[2]	Notes
CHANGE ROW ADDRESS	85h	5	Optional	11h (Optional)	—	—		Yes	5
READ Operations									
READ MODE	00h	0	—	—	—	—		Yes	
READ PAGE	00h	5	—	30h	—	—		Yes	6
READ PAGE MULTI-PLANE	00h	5	—	32h	—	—		Yes	
PROGRAM Operations									
PROGRAM PAGE	80h	5	Yes	10h	—	—		Yes	
PROGRAM PAGE MULTI-PLANE	80h or 81h	5	Yes	11h	—	—		Yes	
PROGRAM SUSPEND	84h	5	—	—	—	—	Yes	Yes	
PROGRAM RESUME	13h	5	—	—	—	—		Yes	
ERASE Operations									
ERASE BLOCK	60h	3	—	D0h	—	—		Yes	
ERASE BLOCK MULTI-PLANE (ONFI)	60h	3	—	D1h	—	—		Yes	
ERASE BLOCK MULTI-PLANE (JEDEC)	60h	3	—	60h	3	D0h		Yes	
ERASE SUSPEND	61h	3	—	—	—	—	Yes	Yes	
ERASE RESUME	D2h	—	—	—	—	—		Yes	
COPYBACK Operations									
COPYBACK READ	00h	5	—	35h	—	—		Yes	6
COPYBACK PROGRAM	85h	5	Optional	10h	—	—		Yes	
COPYBACK PROGRAM MULTI-PLANE	85h	5	Optional	11h	—	—		Yes	

Notes:
1. Busy means RDY = 0.
2. These commands can be used for multi-LUN operations.
3. The READ ID (90h), GET FEATURES (EEh), and GET FEATUERS by LUN (D4h) commands output identical data on rising and falling DQS edges.
4. The SET FEATURES (EFh) and SET FEATURES by LUN (D5h) commands requires data transition prior to the rising edge of CLK, with identical data for the rising and falling edges.
5. Command cycle #2 of 11h is conditional. See CHANGE ROW ADDRESS (85h) for more details.
6. This command can be preceded by up to one READ PAGE MULTI-PLANE (00h-32h) commands, to accommodate a maximum simultaneous two-plane array operation.

Reset Operations

RESET (FFh)

The RESET (FFh) command is used to put a target into a known condition and to abort command sequences in progress. This command is accepted by all LUNs, even when they are busy.

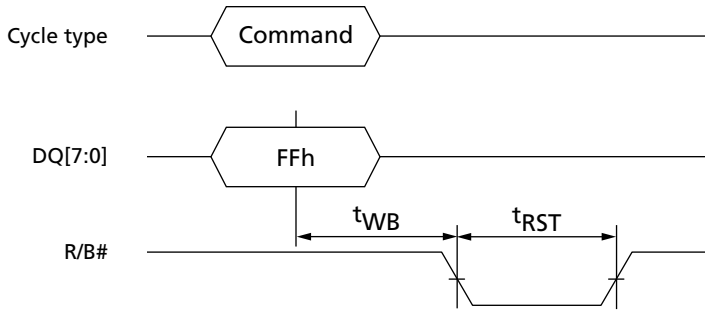
When FFh is written to the command register, the target goes busy for ^{t}RST. During ^{t}RST, the selected target (CE#) discontinues all array operations on all LUNs. All pending single-plane and multi-plane operations are canceled. If this command is issued while a PROGRAM or ERASE operation is occurring on one or more LUNs, the data may be partially programmed or erased and is invalid. The command register is cleared and ready for the next command. The data register and cache register contents are invalid.

RESET must be issued as the first command to each target following power-up (see V_{CC} Power Cycling). Use of the READ STATUS ENHANCED (78h) command is prohibited during the power-on RESET. To determine when the target is ready, use READ STATUS (70h).

If the RESET (FFh) command is issued when the synchronous interface is enabled (NV-DDR/NV-DDR2), the target's interface is changed to the asynchronous interface and the timing mode is set to 0. The RESET (FFh) command can be issued asynchronously when the synchronous (NV-DDR) interface is active, meaning that CLK does not need to be continuously running when CE# is transitioned LOW and FFh is latched on the rising edge of CLK. After this command is latched, the host should not issue any commands during ^{t}ITC. After ^{t}ITC, and during or after ^{t}RST, the host can poll each LUN's status register.

If the RESET (FFh) command is issued when the asynchronous interface is active, the target's asynchronous timing mode remains unchanged. During or after during ^{t}RST, the host can poll each LUN's status register.

Figure 39: RESET (FFh) Cycle



SYNCHRONOUS RESET (FCh)

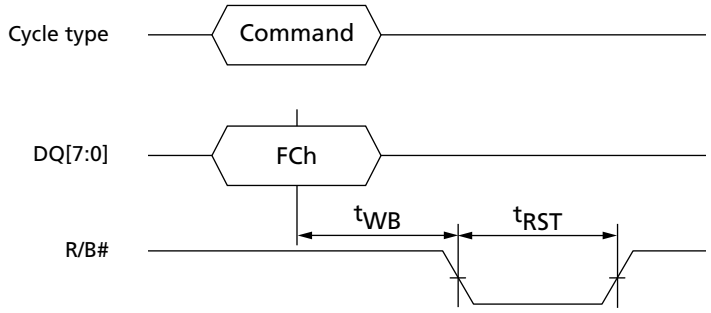
When the synchronous interface is active, the SYNCHRONOUS RESET (FCh) command is used to put a target into a known condition and to abort a command sequence in progress. This command is accepted by all LUNs, even when they are BUSY.

When FCh is written to the command register, the target goes busy for ^{t}RST. During ^{t}RST, the selected target (CE#) discontinues all array operations on all LUNs. All pending single-plane and multi-plane operations are canceled. If this command is issued while a PROGRAM or ERASE operation is occurring on one or more LUNs, the data may be partially programmed or erased and is invalid. The command register is cleared and ready for the next command. The data register and cache register contents are invalid and the synchronous interface remains active.

During or after ^{t}RST, the host can poll each LUN's status register.

SYNCHRONOUS RESET is only accepted while the synchronous interface is active. Its use is prohibited when the asynchronous interface is active.

Figure 40: SYNCHRONOUS RESET (FCh) Operation



RESET LUN (FAh)

The RESET LUN (FAh) command is used to put a particular LUN on a target into a known condition and to abort command sequences in progress. This command is accepted by only the LUN addressed by the RESET LUN (FAh) command, even when that LUN is busy.

When FAh is written to the command register, the addressed LUN goes busy for ^{t}RST. During ^{t}RST, the selected LUN discontinues all array operations. All pending single- and multi-plane operations are canceled. If this command is issued while a PROGRAM or ERASE operation is occurring on the addressed LUN, the data may be partially programmed or erased and is invalid. The command register is cleared and ready for the next command. The data register and cache register contents are valid.

If the RESET LUN (FAh) command is issued when the synchronous (NV-DDR/NV-DDR2) interface is enabled, the targets's interface remains in synchronous mode.

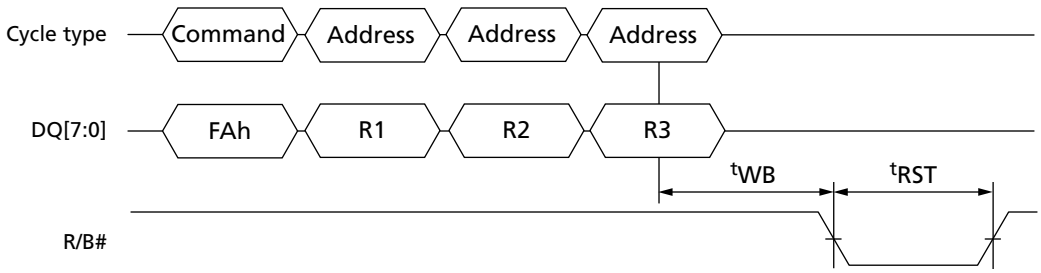
If the RESET LUN (FAh) command is issued when the asynchronous interface is enabled, the target's interface remains in asynchronous mode.

During or after ^{t}RST, the host can poll each LUN's status register.

The RESET LUN (FAh) command is prohibited when not in the default array operation mode.

The RESET LUN (FAh) command can only be issued to a target (CE#) after the RESET (FFh) command has been issued as the first command to a target following power-up.

Figure 41: RESET LUN (FAh) Operation



HARD RESET (FDh)

The HARD RESET (FDh) command is used to put a particular die (LUN) on a target into a known condition similar to that of a power-on initialized state. The HARD RESET (FDh) command is accepted by only the LUN previously selected by a READ STATUS ENHANCED (78h) command. The host is required to issue a READ STATUS ENHANCED (78h) command prior to issuing the HARD RESET (FDh) command, there should be no other NAND commands after the READ STATUS ENHANCED (78h) command and before the HARD RESET (FDh) command issued by the host. The HARD RESET (FDh) command is only permitted to be issued when the selected LUN is not in a busy state (RDY=1, ARDY=1).

HARD RESET (FDh) performs a initialization to the die (LUN) similar to the initialization performed during the first RESET (FFh) command at device power-on. All target LUN parameters and configurations shall be initialized to default values. The target LUN is chosen by the host issuing a READ STATUS ENHANCED (78h) command prior to issuing

the HARD RESET (FDh) command. The HARD RESET (FDh) operation is completed within ^{t}POR. After ^{t}POR, the data register and cache register contents of the previously selected LUN that carried out the HARD RESET (FDh) operation are invalid.

In shared CE# configuration, only the selected LUN shall perform the HARD RESET (FDh) command. The host is required to issue the READ STATUS ENHANCED (78h) command prior to issuing the HARD RESET (FDh) command to select LUN to perform the HARD RESET (FDh) operation.

If in the NV-DDR or NV-DDR2 interface, issuing a HARD RESET (FDh) command will revert the NAND interface back to asynchronous mode and the timing mode is set to 0.

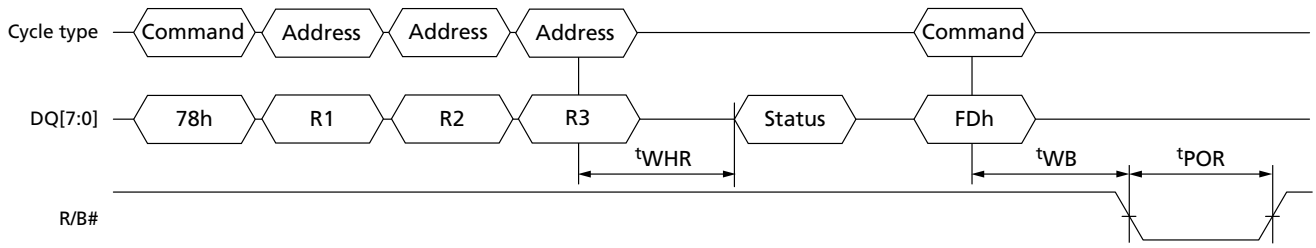
If the HARD RESET (FDh) command is issued when the asynchronous interface is enabled, the target's interface remains in asynchronous mode and timing mode is set to 0.

During or after ^{t}POR, the host can poll each LUN's status register. A status command is only valid 5µs after HARD RESET (FDh) is issued, incorrect status may result if status command is issued within 5µs of HARD RESET (FDh) command.

The HARD RESET (FDh) command is prohibited when not in the default array operation mode.

The HARD RESET (FDh) command can only be issued to a target (CE#) after the RESET (FFh) command has been issued as the first command to a target following power-up. A HARD RESET (FDh) command will not change a device from the mirrored pinout configuration to the non-mirrored pinout configuration or change CE# pin reduction. A HARD RESET (FDh) command will change all feature addresses back to their default values for the target LUN with the exception of previously assigned volume configuration (feature address 58h).

Figure 42: HARD RESET (FDh) Operation



Identification Operations

READ ID (90h)

The READ ID (90h) command is used to read identifier codes programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing 90h to the command register puts the target in read ID mode. The target stays in this mode until another valid command is issued.

When the 90h command is followed by a 00h address cycle, the target returns a 5-byte identifier code that includes the manufacturer ID, device configuration, and part-specific information.

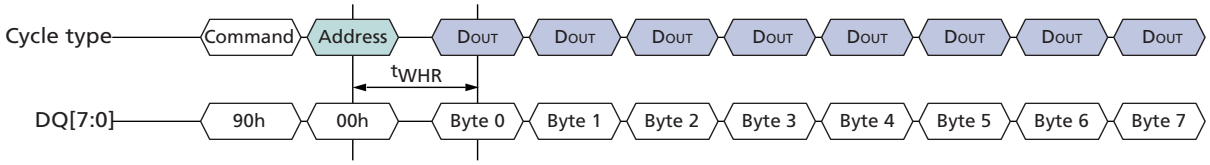
When the 90h command is followed by a 20h address cycle, the target returns the 6-byte ONFI identifier code.

When the 90h command is followed by a 40h address cycle, the target returns the 5-byte JEDEC identifier code.

After the 90h and address cycle are written to the target, the host enables data output mode to read the identifier information. When the asynchronous interface is active, one data byte is output per RE# toggle. When the NV-DDR interface is active, one data byte is output per rising edge of DQS when ALE and CLE are HIGH; the data byte on the falling edge of DQS is identical to the data byte output on the previous rising edge of DQS. When the NV-DDR2 interface is active, one data byte is output per rising edge of DQS when ALE and CLE are LOW; the data byte on the falling edge of DQS is identical to the data byte output on the previous rising edge of DQS.

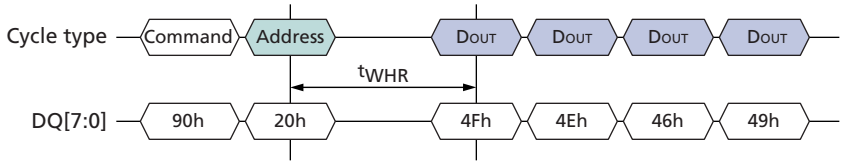
If host issues READ ID (90h) command during a program data load sequence, first the data load sequence must be closed and internal pipeline flushed with an 11h command prior to issuing the command.

Figure 43: READ ID (90h) with 00h Address Cycle Operation



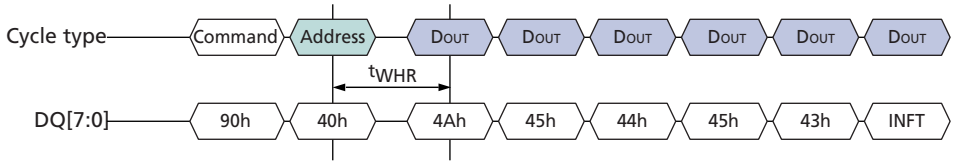
Notes: 1. See READ ID Parameter Tables for byte definitions.

Figure 44: READ ID (90h) with 20h Address Cycle Operation



Notes: 1. See READ ID Parameter Tables for byte definitions.

Figure 45: READ ID (90h) with 40h Address Cycle Operation



Notes: 1. See READ ID Parameter Tables for byte definitions.

READ ID Parameter Tables

Table 14: READ ID Parameters for Address 00h

Device	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
FxxL05Bxxxxxxx	2Ch	84h	44h	32h	AAh	04h	00h	00h

Notes: 1. h = hexadecimal.

Table 15: READ ID Parameters for Address 20h

Device	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
FxxL05Bxxxxxxx	4Fh	4Eh	46h	49h	00h

Notes: 1. h = hexadecimal.

READ PARAMETER PAGE (ECh)

The READ PARAMETER PAGE (ECh) command is used to read the ONFI or JEDEC parameter page programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing ECh to the command register puts the target in read parameter page mode. The target stays in this mode until another valid command is issued.

When the ECh command is followed by an 00h or 40h address cycle, the target goes busy for ^{t}R. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode. Use of the READ STATUS ENHANCED (78h) command is prohibited while the target is busy and during data output.

After ^{t}R completes, the host enables data output mode to read the parameter page. When the asynchronous interface is active, one data byte is output per RE# toggle. When the synchronous interface is active, one data byte is output for each rising or falling edge of DQS.

A minimum of three copies of the parameter page are stored in the device. Each parameter page is 256 bytes. If desired, the CHANGE READ COLUMN (05h-E0h) command can be used to change the location of data output. Use of the CHANGE READ COLUMN ENHANCED (06h-E0h or 00h-05h-E0h) command is prohibited.

The READ PARAMETER PAGE (ECh) output data can be used by the host to configure its internal settings to properly use the NAND Flash device. Parameter page data is static per part, however the value can be changed through the product cycle of NAND Flash. The host should interpret the data and configure itself accordingly.

The host should continue reading redundant parameter pages until the host is able to accurately reconstruct the parameter page contents. Parameter pages returned by the target may have invalid CRC values; however, bit-wise majority may be used to recover the contents of the parameter page. The host may use bit-wise majority or other techniques to recover the contents of the parameter page from the parameter page copies present.

Figure 46: READ PARAMETER (ECh) with 00h Address Operation for ONFI

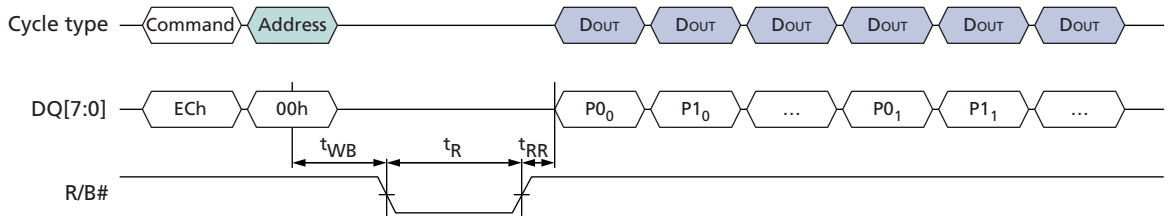
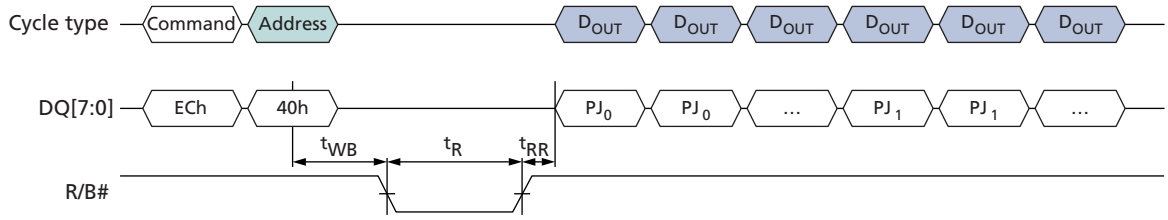


Figure 47: READ PARAMETER (ECh) with 40h Address Operation for JEDEC



Configuration Operations

The SET FEATURES (EFh) and GET FEATURES (EEh) commands are used to modify the target's default power-on behavior. These commands use a one-byte feature address to determine which subfeature parameters will be read or modified. Each feature address (in the 00h to FFh range) is defined in Table 16. The SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command writes subfeature parameters (P1-P4) to the specified feature address. The GET FEATURES (EEh) or GET FEATURES by LUN (D4h) command reads the subfeature parameters (P1-P4) at the specified feature address.

Unless otherwise specified, the values of the feature addresses do not change when RESET (FAh, FFh, FCh) is issued by the host. A HARD RESET (FDh) command will reset all feature addresses to their default values for the target LUN. A HARD RESET (FDh) command will not undo any previously set electronic mirroring, CE# pin reduction, or volume addressing assignments that were performed prior to the HARD RESET (FDh) command.

Table 16: Feature Address Definitions

Feature Address	Definition
00h	Reserved
01h	Timing mode
02h	NV-DDR2 configuration
03h–0Fh	Reserved
10h	Programmable output drive strength
11h–57h	Reserved
58h	Volume configuration
59h–7Fh	Reserved
80h	Programmable output drive strength
81h	Programmable RB# pull-down strength
82h–88h	Reserved
89h	Read Retry
8Ah–8Fh	Reserved
90h	Array operation mode
91h	SLC MODE operation
92h–E5h	Reserved
E6h	Sleep Mode
E7h	Temperature sensor
E8h–F4h	Reserved
F5h	Snap read/Express read
F6h	Sleep Rite
F7h–FFh	Reserved

SET FEATURES EFh

The SET FEATURES (EFh) command writes the subfeature parameters (P1-P4) to the specified feature address to enable or disable target-specific features. This command is accepted by the target only when all die (LUNs) on the target are idle.

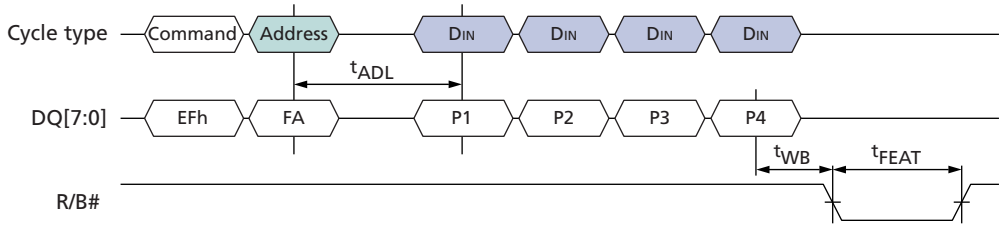
Writing EFh to the command register puts the target in the set features mode. The target stays in this mode until another command is issued.

The SET FEATURES (EFh) command is followed by a valid feature address as specified in Table 16. The host waits for tADL before the subfeature parameters are input. When the asynchronous interface is active, one subfeature parameter is latched per rising edge of WE#. When the NV-DDR or NV-DDR2 interface is active, one subfeature parameter is latched per rising edge of DQS_t. The data on the falling edge of DQS_t should be identical to the subfeature parameter input on the previous rising edge of DQS_t. The device is not required to wait for the repeated data byte before beginning internal actions.

After all four subfeature parameters are input, the target goes busy for tFEAT, unless otherwise specified. The READ STATUS (70h) command can be used to monitor for command completion.

Feature address 01h (Timing mode) operation is unique. If SET FEATURES is used to modify the interface type, the target will be busy for tITC. See Activating Interfaces for details.

Figure 48: SET FEATURES (EFh) Operation



GET FEATURES (EEh)

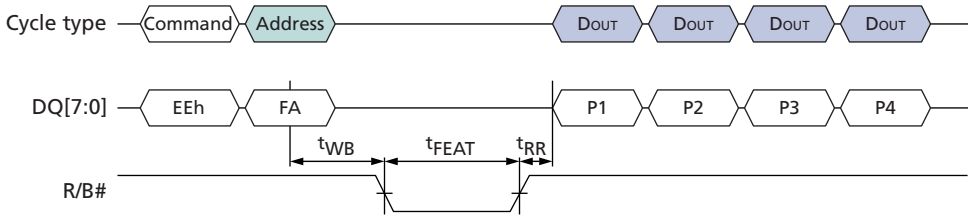
The GET FEATURES (EEh) command reads the subfeature parameters (P1-P4) from the specified feature address. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing EEh to the command register puts the target in get features mode. The target stays in this mode until another valid command is issued.

When the GET FEATURES (EEh) command is followed by a feature address, the target goes busy for tFEAT, unless otherwise specified. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode. During and prior to data output, use of the READ STATUS ENHANCED (78h) command is prohibited.

After tFEAT completes, the host enables data output mode to read the subfeature parameters. When the asynchronous interface is active, one data byte is output per RE# toggle. When the NV-DDR or NV-DDR2 interface is active, one subfeature parameter is output per DQS_t toggle on rising or falling edge of DQS_t.

Figure 49: GET FEATURES (EEh) Operation



GET/SET FEATURES by LUN (D4h/D5h)

The original GET FEATURES (EEh) and SET FEATURES (EFh) commands were target (CE#) based operations that did not take into account LUN addressing. By that, setting a feature address or getting a value for a feature address for a given target (CE#) applied to all LUNs on that target (CE#). GET FEATURES by LUN (D4h) and SET FEATURES by LUN (D5h) commands have the ability to also select a LUN address gives added flexibility to set the same feature address to different values for each LUN on a target (CE#) for more complex and versatile system solutions.

GET FEATURES by LUN (D4h) and SET FEATURES by LUN (D5h) operations work in the same manner as the non-LUN versions of those commands that did not take LUN addressing into account. The GET FEATURES by LUN (D4h) and SET FEATURES by LUN (D5h) commands both have an added LUN address cycle that is before the address cycle of the feature address which denotes the LUN to select for the operation. See Table 17 for the decode of the LUN address cycle.

Table 17: GET/SET FEATURES by LUN Operation LUN Address Cycle Decoding

Description	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
LUN											
LUN selection	LUN0								0	0b	
	LUN1								1	1b	
Reserved	–	–	–	–	–	–	–	–			

GET FEATURES by LUN (D4h) and SET FEATURES by LUN (D5h) can be issued to any addressable LUN that is not busy (RDY = 1, ARDY = 1). Target LUN status can be determined by using the READ STATUS ENHANCED (78h) command. When doing multiple LUN operations, refer to the Interleaved Die (Multi-LUN) Operation section for details on proper operations.

Figure 50: GET FEATURES by LUN (D4h) Operation

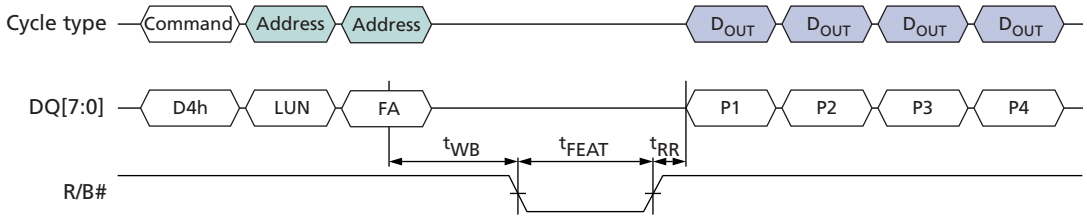


Figure 51: SET FEATURES by LUN (D5h) Operation

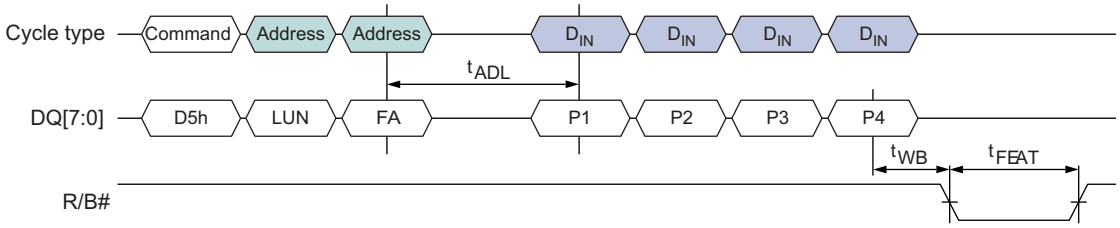


Table 18: Feature Address 01h: Timing Mode

Sub-Feature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Timing mode	Mode 0 (default)					0	0	0	0	x0h	1, 2, 3
	Mode 1					0	0	0	1	x1h	
	Mode 2					0	0	1	0	x2h	
	Mode 3					0	0	1	1	x3h	
	Mode 4					0	1	0	0	x4h	
	Mode 5					0	1	0	1	x5h	
	Mode 6					0	1	1	0	x6h	
	Mode 7					0	1	1	1	x7h	
	Mode 8					1	0	0	0	x8h	
	Mode 9					1	0	0	1	x9h	
	Mode 10					1	0	1	0	xAh	
	Reserved					1	X	X	X	Bh–Fh	
Data interface	Asynchronous (default)			0	0					0xh	1
	NV-DDR			0	1					1xh	
	NV-DDR2			1	0					2xh	
	Reserved			1	1					3xh	
Program clear	Program command clears all cache registers on a target (default)		0							0b	
	Program command clears only addressed LUN cache register on a target		1							1b	
Reserved		0								0b	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes: 1. Asynchronous timing mode 0 is the default, power-on value when the NAND device is powered-on with V_{CCQ} in the 1.8V operational range.
2. If the NV-DDR or NV-DDR2 interface is active, a RESET (FFh) command will change the timing mode and data interface bits of feature address 01h to their default values. If the asynchronous interface is active, a RESET (FFh) command will not change the values of the timing mode or data interface bits to their default valued. Transition from the NV-DDR interface to the NV-DDR2 interface or vice versa is not permitted.

Table 19: Feature Address 02h: NV-DDR2 configuration

Sub-Feature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Voltage Reference (VEN)	External V_{REFQ} is disabled and internal voltage is used as reference for DQ signals (default)								0	0b	1, 2
	External V_{REFQ} is enabled and used as reference for DQ signals								1	1b	
Complementary DQS (CMPD)	DQS_c signal disabled (default)							0		0b	
	DQS_c signal enabled							1		1b	
Complementary RE# (CMPR)	RE_c signal disabled (default)						0			0b	
	RE_c signal enabled						1			1b	
Reserved	–					0				0b	
DQ[7:0],DQS_t, DQS_c, RE_t, and RE_c ODT enable	ODT disabled (default)	0	0	0	0					0h	3
	ODT enabled with R_{TT} of 150 Ohms	0	0	0	1					1h	
	ODT enabled with R_{TT} of 100 Ohms	0	0	1	0					2h	
	ODT enabled with R_{TT} of 75 Ohms	0	0	1	1					3h	
	ODT enabled with R_{TT} of 50 Ohms	0	1	0	0					4h	
	Reserved	0	1	0	1					5h	
		0	1	1	0					6h	
		0	1	1	1					7h	
		1	X	X	X					8h–Fh	
P2											
Warmup RE_t/RE_c and DQS cycles for data output	0 cycles (default)					0	0	0	0	0h	4
	1 warmup cycle					0	0	0	1	1h	
	2 warmup cycle					0	0	1	0	2h	
	3 warmup cycle					0	0	1	1	3h	
	4 warmup cycle					0	1	0	0	4h	
	Reserved					0	1	0	1	5h	
						0	1	1	0	6h	
						0	1	1	1	7h	
						1	X	X	X	8h–Fh	

Table 19: Feature Address 02h: NV-DDR2 configuration (Continued)

Sub-Feature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Warmup DQS cycles for data input	0 cycles (default)	0	0	0	0					0h	5
	1 warmup cycle	0	0	0	1					1h	
	2 warmup cycle	0	0	1	0					2h	
	3 warmup cycle	0	0	1	1					3h	
	4 warmup cycle	0	1	0	0					4h	
	Reserved	0	1	0	1					5h	
		0	1	1	0					6h	
		0	1	1	1					7h	
		1	X	X	X					8h–Fh	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes:
1. If set to one, then external V_{REFQ} is used as a reference for the input and I/O signals. If cleared to zero, then internal V_{REFQ} is used as a reference for the input and I/O signals. This setting applies to input and I/O signals, including DQ[7:0], DQS_t, DQS_c, RE_t, RE_c, WE#, ALE, and CLE. CE# and WP# are CMOS signals and always use internal V_{REFQ}.
2. If the NV-DDR2 interface is active, a RESET (FFh) command will change the bit values feature address 02h to their default values.
3. This field controls the on-die termination settings for the DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c signals. R_{TT} settings may be specified separately for DQ[7:0]/DQS and the RE# signals. The DQ[7:0]/DQS may be specified separately for data input versus data output operation. Refer to the definition of the ODT CONFIGURE (E2h) command. If values are specified with the ODT CONFIGURE (E2h) command, then this field is not used. GET FEATURES (EEh) returns the previous value set in this field, regardless of the R_{TT} settings specified using ODT CONFIGURE (E2h).
4. Number of warmup cycles for DQS and RE_t/RE_c and DQS_t/DQS_c for data output. The number of initial "dummy" RE_t/RE_c cycles at the start of data output operations. There are corresponding "dummy" DQS_t/DQS_c cycles to the "dummy" RE_t/RE_c cycles that the host shall ignore during data output.
5. This field indicates the number of warmup cycles of DQS that are provided for data input. These are the number of initial "dummy" DQS_t/DQS_c cycles at the start of data input operations.

Table 20: Feature Addresses 58h: Volume configuration

Sub-Feature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Volume Address	Field used to assign a value for a given Volume Address					X	X	X	X		1
Reserved		0	0	0	0					0h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Note: 1. After the Volume Address is appointed, the ENo pin for that Volume is set to one, the ENi pin for that Volume is ignored until the next power cycle, and the Volume is deselected until a VOLUME SELECT (E1h) command is issued that selects the associated Volume. The host shall only set this feature once per power cycle for each Volume. The address specified is then used in VOLUME SELECT (E1h) command for accessing this NAND Target. This setting is retained across RESET (FAh, FCh, FFh) commands.

Table 21: Feature Addresses 10h and 80h: Programmable Output Drive Strength

Sub-Feature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Output drive strength	Not supported							0	0	00h	1
	25 Ohms							0	1	01h	
	35 Ohms (default)							1	0	02h	
	50 Ohms							1	1	03h	
Reserved		0	0	0	0	0	0			00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Note: 1. See Output Drive Impedance for details.

Table 22: Feature Addresses 81h: Programmable R/B# Pull-Down Strength

Sub-Feature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
R/B# pull-down strength	Full (default)							0	0	00h	1
	Three-quarter							0	1	01h	
	One-half							1	0	02h	
	One-quarter							1	1	03h	
Reserved		0	0	0	0	0	0			00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes: 1. This feature address is used to change the default R/B# pull-down strength. Its strength should be selected based on the expected loading of R/B#. Full strength is the default, power-on value.

Table 23: Feature Addresses 89h: Read Retry

Sub-Feature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Read Retry	Disable (default)					0	0	0	0	00h	
	Option 1					0	0	0	1	01h	
	Option 2					0	0	1	0	02h	
	Option 3					0	0	1	1	03h	
	Option 4					0	1	0	0	04h	
	Option 5					0	1	0	1	05h	
	Option 6					0	1	1	0	06h	
	Option 7					0	1	1	1	07h	
	Option 8					1	0	0	0	08h	2
	Option 9					1	0	0	1	09h	
	Option 10					1	0	1	0	0Ah	
	Option 11					1	0	1	1	0Bh	
	Option 12					1	1	0	0	0Ch	
	Option 13					1	1	0	1	0Dh	
	Option 14					1	1	1	0	0Eh	
	Option 15					1	1	1	1	0Fh	
Reserved		0	0	0	0					00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											

Table 23: Feature Addresses 89h: Read Retry

Sub-Feature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Reserved		0	0	0	0	0	0	0	0	00h	

Notes: 1. See Read Retry Operations for details.
2. ^{t}R will be longer with selected option. See Electrical Specification – Array Characteristics section for details.

Table 24: Feature Addresses 90h: Array Operation Mode

Sub-Feature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Array Operation Mode	Normal (default)								0	00h	
	OTP Block								1	01h	
Reserved		0	0	0	0	0	0	0		00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes: 1. A RESET (FFh/FCh) command will cause the bits of the array operation mode to change to their default values. If in NV-DDR/NV-DDR2 mode, a SYNCHRONOUS RESET (FCh) command will cause the bits for the array operation mode to change to their default values.

Table 25: Feature Addresses E6h: Sleep Mode

Sub-Feature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Sleep mode	Sleep mode disabled (default)								0	0b	
	Sleep mode enabled								1	1b	
	Sleep_V_{CCQ} mode disabled (default)							0		0b	
	Sleep_V_{CCQ} mode enabled							1		1b	
Reserved	–	–	–	–	–	–	–			–	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Sleep mode is a power state in which the LUNs power consumption is minimal. Sleep_V_{CCQ} mode is a power state in which V_{CCQ} can be removed to reduce I_{SBQ}. The trade off for this functionality is longer wake up duration from the Sleep and/or Sleep_V_{CCQ} state.

The die (LUN) will retain its entire configuration (including Set Feature settings, RV level values, etc.) during Sleep mode, but does not retain the contents of the cache or data registers. During Sleep_V_{CCQ} mode the die will retain its entire configuration (including settings, RV level values, etc) and the contents of the cache or data registers.

Sleep Mode is enabled by issuing a SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to feature address E6h. After the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command is issued, the target (CE#) or target LUN will enter Sleep mode upon bringing CE# HIGH. The target (CE#) or target LUN will enter Sleep_V_{CCQ} mode when CE# is brought HIGH and V_{CCQ} is powered down. Powering down V_{CCQ} is a requirement to enter Sleep_V_{CCQ}. Both Sleep and Sleep_V_{CCQ} modes can be entered simultaneously or separately.

During Sleep mode, upon asserting CE# LOW, the LUN will exit the mode and change state to Normal mode. During Sleep_V_{CCQ} mode or when both Sleep and Sleep_V_{CCQ} modes are entered, upon asserting CE# LOW and issuing the RESET (FFh) command, the LUN will exit the current sleep mode(s) and change state to Normal mode. The transition period between Sleep Mode and Normal Mode shall be less than ^{t}SLP. After the transition, the LUN will move to Normal Ready mode and be ready to receive commands. When exiting from Sleep_V_{CCQ} mode the host is required to issue a RESET (FFh) command to the LUN. If both Sleep and Sleep_V_{CCQ} modes are entered the host is required to issue a RESET (FFh) command to the LUN and the ^{t}RST time associated with that RESET (FFh) command will be equivalent to ^{t}SLP.

For a configuration of more than one LUN sharing the same CE# (or Volume Address), if SET FEATURES (EFh) command is used to enter Sleep and/or Sleep_V_{CCQ} mode(s), the shared LUNs shall jointly enter/exit to/from Sleep/Sleep_V_{CCQ} mode. All LUNs on a target (CE#) shall monitor in parallel the SET FEATURES (EFh) or SET FEATURE by LUN (D5h) command to enter the mode. As CE# is shared, upon asserting the signal, all LUNs on a target shall exit from Sleep Mode. Upon issuing the RESET (FFh)) command to LUNs that share a CE#, all LUNs shall exit form Sleep_V_{CCQ} (or Sleep/Sleep_V_{CCQ}) mode.

For Sleep mode, it is not required to have all targets (CE#s) of a NAND device enabled for Sleep mode. A host can have as little as LUN enabled for Sleep mode. For Sleep_V_{CCQ} mode, it is required to have all devices that share a common V_{CCQ} enabled for Sleep_V_{CCQ} mode prior to removing V_{CCQ} from the NAND device.

Once Sleep mode is entered, the host is required to keep the NAND device in Sleep mode for a minimum time of 1µs before exiting Sleep mode.

The host shall not issue any commands with exception of RESET (FFh, FAh, FCh, FDh) between issuing the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to enable Sleep mode (Feature Address E6h) and bringing CE# HIGH to enter Sleep mode. The host shall not issue any commands between issuing the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to enable Sleep_V_{CCQ} mode (i.e. Feature Address E6h, P1[1]=1) and bringing CE# HIGH and powering down V_{CCQ} to enter Sleep_V_{CCQ} mode

When V_{CCQ} = 0V, the host must keep RE_t/RE_c, DQS_t/DQS_c signals LOW. RE_t/RE_c, DQS_t/DQS_c signals maybe ramped with V_{CCQ} during power up but not exceed V_{CCQ}. When V_{CCQ} = 0V, the host must keep DQ[7:0] signals LOW or they can be left Hi-Z. DQ[7:0] signals maybe ramped with V_{CCQ} during power up but not exceed V_{CCQ}.

If a RESET (FFh, FAh, FCh, FDh) command is issued to the target (CE#) or LUN after a SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to enable Sleep mode is issued, but before CE# goes HIGH, the target (CE#) or LUN will not enter Sleep Mode upon CE# HIGH. In other words, the setting for Sleep mode is not retained across RESET (FFh, FAh, FCh, FDh) operations. If Sleep and Sleep_V_{CCQ} are both entered with SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command, no commands are allowed to be issued to the NAND until after V_{CCQ} is powered down and then powered back up. If Sleep_V_{CCQ} mode is entered with SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command, any commands issued to the NAND device, including RESET (FFh, FAh, FCh, FDh), will be ignored until after V_{CCQ} power is removed.

When exiting Sleep mode or when exiting with both Sleep and Sleep_V_{CCQ} modes enabled, CE# shall be asserted LOW for a minimum of ^{t}CE_SLP.

When exiting Sleep Mode, the host is required to wait ^{t}SLP before issuing any commands (including RESET) to the device. During ^{t}SLP period the device may draw significantly more current than I_{SB} even when CE# is HIGH. When exiting Sleep/Sleep_V_{CCQ} mode, the host is required to wait ^{t}SLP after issuing RESET (FFh) command to exit the mode. During this ^{t}SLP period, the device may draw significantly more current than I_{SB} even when CE# is HIGH.

Table 26: Sleep Mode Parameters

Parameter	Min	Max	Units
^{t}SLP	–	50	µs
^{t}CE_SLP	–	200	ns
Sleep_V_{CCQ} exit (^{t}RST)	–	10	µs
Sleep and Sleep_V_{CCQ} exit (^{t}RST)	–	50	µs
CE# LOW exiting Sleep or Sleep_V_{CCQ}	200	–	ns
V_{CCQ} time to be <100mV during Sleep_V_{CCQ} mode	25	–	ns
$I_{SB\_SLEEP/SLEEP\_VCCQ}$	–	20	µA
I_{SBQ_SLEEP}	–	25	µA
$I_{SBQ\_SLEEP\_VCCQ}$	–	0	µA

Sleep mode entry/exit required method:

1. Issue a SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to feature address E6h with subfeature P1 = 1h to enable Sleep mode entry.
2. CE# is brought HIGH after Sleep mode entry and the NAND target (CE#) enters Sleep mode.
3. CE# is brought LOW to exit Sleep mode. Sleep mode entry is cleared (for example, DQ0 of subfeature P1 of feature address E6h is automatically cleared).
4. During the ^{t}SLP time allowed for the NAND target to return to normal mode from Sleep mode. no commands (including RESET) are allowed to the target.
5. To re-enter Sleep mode the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to feature address E6h with subfeature P1 = 1h to enable Sleep mode entry must be issued again.

Sleep_V_{CCQ} entry/exit required method:

1. Issue a SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to feature address E6h with subfeature P1 = 2h to enable Sleep_V_{CCQ} mode entry.
2. CE# is brought HIGH and then V_{CCQ} is removed after Sleep_V_{CCQ} mode entry has been selected and the device enters Sleep_V_{CCQ} mode. Once the host issues SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to feature address E6h to

enter Sleep_V_{CCQ} mode, the host must execute a power cycle on V_{CCQ} before any command may be entered. User is required bring V_{CCQ} below 100mV for at least 25µs. While V_{CCQ} is powered down R/B#, DQs, and DQS signals shall be left floating or cannot be driven higher than 0V.

3. V_{CCQ} is powered-on. When powering up V_{CCQ}, the host is required to follow V_{CCQ} power on requirements and no input signal transitions shall occur when ramping V_{CCQ} and V_{CCQ} <0.85V. The device stays in the interface configured when Sleep_V_{CCQ} mode was entered.
4. The host shall issue a RESET (FFh) command to the NAND device to exit Sleep_V_{CCQ} mode. The Sleep_V_{CCQ} mode entry is cleared (for example, the SET Feature Bit for Sleep mode entry is automatically cleared). The ^{t}RST time for the RESET (FFh) command is within ^{t}RST (for example, no NAND trims are loaded as they were maintained during Sleep_V_{CCQ} mode).
5. To re-enter Sleep_V_{CCQ} mode the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to feature address E6h with subfeature P1 = 2h to enabled Sleep_V_{CCQ} mode entry must be issued again.

Sleep and Sleep_V_{CCQ} entry/exit required method:

1. Issue a SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to feature address E6h with subfeature P1 = 3h to enable Sleep and Sleep_V_{CCQ} mode entry.
2. CE# is brought HIGH and then V_{CCQ} is removed after Sleep/Sleep_V_{CCQ} mode entry and the device enters both Sleep and Sleep_V_{CCQ} mode. Once the user issues SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to enter Sleep/Sleep_V_{CCQ} mode, the host must execute a power cycle on V_{CCQ} before any command may be entered. The host is required bring V_{CCQ} below 100mV for at least 1µs. While V_{CCQ} is powered down R/B#, DQs, and DQS signals shall be left floating or cannot be driven higher than 0V.
3. To exit Sleep and Sleep_V_{CCQ} mode, V_{CCQ} is powered-on. When powering-up V_{CCQ}, the host is required to follow V_{CCQ} power-on requirements and no input signal transitions shall occur when ramping V_{CCQ} and V_{CCQ} <0.85V. The device stays in the interface configured when Sleep/Sleep_V_{CCQ} was entered.
4. The host shall issue a RESET (FFh) command to all targets (CE#s) of the NAND device to exit Sleep_V_{CCQ} mode. The Sleep_V_{CCQ} mode entry is cleared (for example, the SET Feature Bit for Sleep mode entry is automatically cleared). The ^{t}RST time for the RESET (FFh) command is up to ^{t}SLP (for example, no NAND trims are loaded as they were maintained during Sleep/Sleep_V_{CCQ} mode).
5. During the ^{t}SLP time allowed for the NAND target to return to normal mode from Sleep/Sleep_V_{CCQ} mode. no commands (including RESET) are allowed to the target.
6. To re-enter Sleep/Sleep_V_{CCQ} mode the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to feature address E6h with subfeature P1 = 3h to enabled Sleep/Sleep_V_{CCQ} mode entry must be issued again.

Table 27: Feature Addresses E7h: Temperature Sensor Readout

Sub-Feature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Temperature sensor readout	-37°C example output		0	0	0	0	0	0	0	00h	1, 2
	-35.8°C example output		0	0	0	0	0	0	1	01h	
	–		X	X	X	X	X	X	X	–	
	89°C example output		1	1	0	1	0	0	1	69h	
	90.2°C example output		1	1	0	1	0	1	0	6Ah	
	Reserved		–	–	–	–	–	–	–	6Bh–7Fh	
Reserved		0								0b	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes: 1. Each bit is roughly 1.2°C. For example, an output of 55h is roughly 65°C.
2. Device reading out temperature beyond specified operational temperature ranges for a given device is not meant to signify support of those temperatures.

Only a GET FEATURES (EEh) or GET FEATURES by LUN (D4h) commands are permitted to feature address E7h, SET FEATURES (EFh) and SET FEATURES by LUN (D5h) commands are not supported to feature address E7h. The temperature sensor shall return the current temperature value no more than ^{t}TEMP after the host controller issues the GET FEATURES (EEh) or GET FEATURES by LUN (D4h) command to feature address E7h. GET FEATURES (EEh) and GET FEATURES by LUN (D4h) commands are not supported to feature address E7h when the target (CE#) or target LUN is in any busy state.

If there is only 1 LUN per CE# of a NAND device, then either the GET FEATURES (EEh) or GET FEATURES by LUN (D4h) command can be used to access the temperature sensor readout (feature address E7h). If there is more than one LUN per CE#, then the GET FEATURES by LUN (D4h) command shall be used to access the temperature sensor readout (feature address E7h), not the GET FEATURES (EEh) command, to avoid possible data contention.

Table 28: Feature Addresses F5h: Snap Read/Express Read

Sub-Feature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P10b											
Snap read/Express read enable	Reserved								0	0b	
	Snap read/Express read disable (default)						0	0		00b	
	Express read enable						0	1		01b	
	Snap read enable						1	1		11b	
	Reserved	0	0	0	0	0				00000 b	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

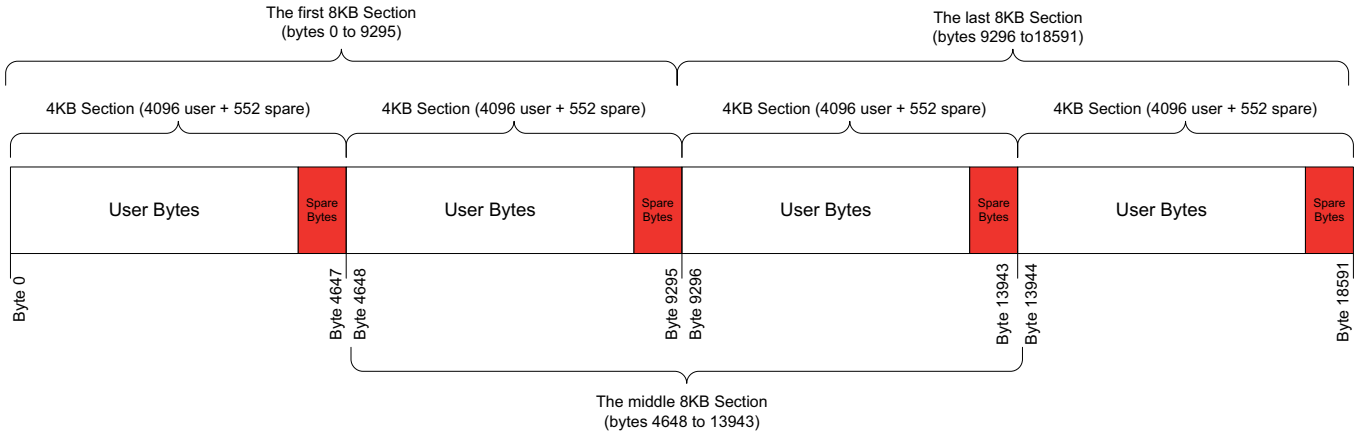
Feature address F5h: Snap read/Express read controls two different feature configurations. The snap read feature provides fastest possible read of a partial page. The express read feature allows the host to begin clocking out data before the READ command has fully completed, also allowing for faster ^{t}R for READ operations with internal NAND randomizer disabled. A snap read includes express read functionality.

Note that snap read cannot be used in conjunction with the NAND internal data randomizer. If performing a snap read from a page that has been programmed with the NAND internal randomizer enabled, indeterminate data will be output.

The snap read feature allows for a fixed 8KB+ section of a page to be read, providing fastest possible ^{t}R times.

When the Snap Read feature is enabled, all read operations will occur within a fixed 8K+ section of a page. The page has 3 fixed 8KB+ logical sections: bytes 0 - 9295, bytes 4648 - 13943, and bytes 9296 - 18591 (each section contains 2 x 4KB sections plus 2 x ¼ of the spare area bytes). When any read command is issued, the byte address specified by the command will determine which section of the page to be read. It is not necessary to address the first byte in a particular section during a read operation. Addressing any byte within the first 4KB+ section (bytes 0 - 4647) will activate the first 8KB+ section (bytes 0 - 9295); Addressing any byte within the second 4KB+ section (bytes 4648 - 9295) will activate the middle 8KB+ section (bytes 4648 - 13943); Addressing any byte within the third or fourth 4KB+ sections (bytes 9296 - 13843 or bytes 13944 - 18591) will activate the last 8KB+ section (bytes 9296 - bytes 18591). When using the NV-DDR2 interface, CA0 is forced to 0 internally, so start byte address is always an even byte. Data will be invalid for byte addresses not included in the selected 8KB+ section of the page.

Figure 52: Example of Fixed 8kB+ Length Sections



Snap read is only performed if READ PAGE (00h - 30h) is issued to the device. If READ PAGE MULTI-PLANE (00h-32h) or feature address 89h: Read retry options selected that has a longer ^{t}R time are issued to the device, the snap read is not executed and the commands issued are executed.

Snap read is not supported if reading from a page where not all shared pages have been programmed (for example, not in full MLC “4” state). In this case, undetermined data will result.

Snap read is supported in erase suspend or program suspend state.

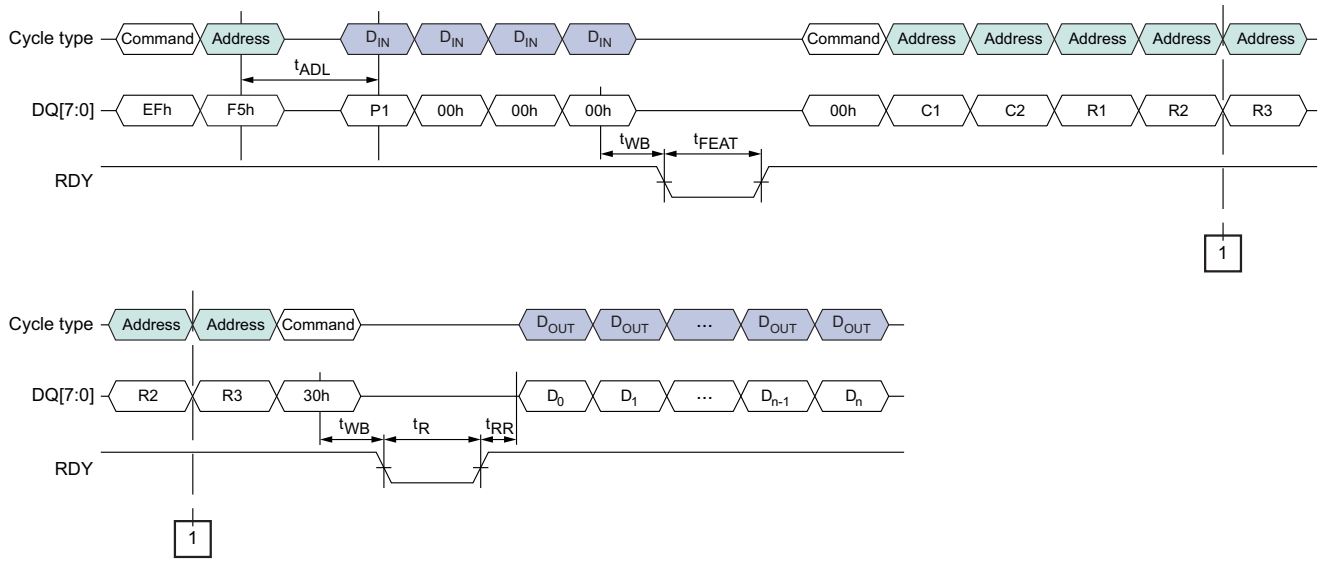
Snap read should not be used to check for bad blocks when building a bad block table.

Snap read is only supported in the case of SINGLE-PLANE READ operations.

READ UNIQUE ID (EDh), READ OTP PAGE, and READ PARAMETER PAGE (ECh) commands are issued to the device the snap read is not executed and the commands are executed.

Snap read incorporates the express read feature, so any express read requirements must also be met for snap read.

Figure 53: Example of Snap Read Sequence



Note: Byte address of data byte D_0 is defined by the byte addressed by C1 and C2.

The express read feature allows the host to begin clocking data out of the part once the data in the data register becomes valid. This will happen before the entire read algorithm is completed, thus reducing the apparent ^{t}R time for READ operations with internal NAND randomizer disabled. Before any additional array commands can be issued the entire read algorithm must be completed. Express read is not optimized to provide ^{t}R savings with WL flag status read enabled.

When the express read feature is enabled the host must monitor the status register using either READ STATUS (70h) or READ STATUS ENHANCED (78h) commands. Status register bit 6 ('RDY') will provide a method for the host to determine when data can begin being clocked out of the device. Status register bit 5 ('ARDY') will remain LOW until the entire read algorithm has been completed. The host must not issue any additional array operations until status register bit 5 is ready. In addition to read status (70h/78h) and RESET (FFh/FCh/FAh) commands, the host is allowed to issue the CHANGE READ COLUMN (05h-E0h), CHANGE READ COLUMN ENHANCED (06h- E0h/00h-05h-E0h), READ PAGE MULTI-PLANE (00h-32h), PAGE READ (00h-30h), and READ MODE (00h) commands when status register bit 5 ('ARDY') is LOW and status register bit 6 ('RDY') is HIGH during express read.

Express read may be enabled for any read command, but in some cases Express Read will not be executed and no ^{t}R improvement witnessed. If express read is enabled when corrective read (FA = 93h) or auto read calibration (FA = 96h) is also enabled, express read will not be executed and no ^{t}R improvement witnessed.

Figure 54: Example of Express Read Sequence

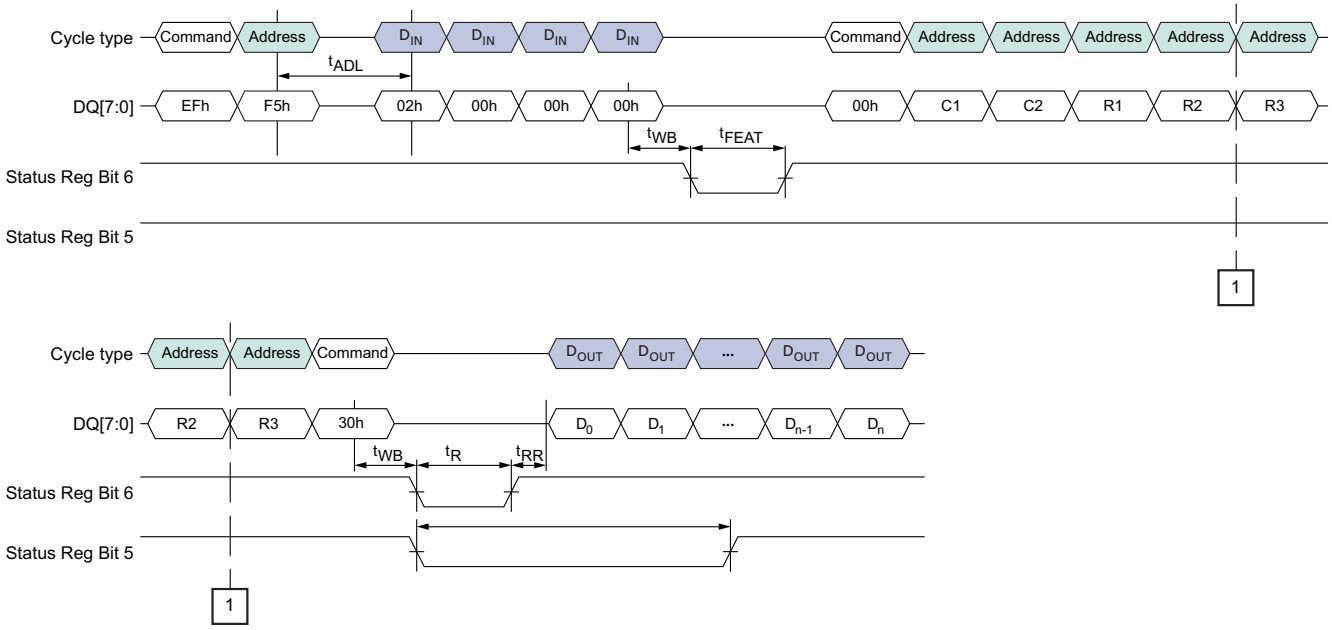


Table 29: Feature Addresses F6h: Sleep Lite

Sub-Feature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Sleep lite configuration	Sleep lite disable (default)							0	0	00b	
	Sleep lite enable							0	1	01b	
	Sleep lite – target level enable							1	1	11b	
	Reserved	–	–	–	–	–	–				
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

The sleep lite feature allows the host to place unselected LUNs on an active target (CE#) into a low power state to reduce overall I_{CC} where the current consumption by any LUN in sleep lite will be I_{SB} and I_{SBQ}. This feature only applies to NAND targets where more than one LUN exists per CE#. Once a LUN has been placed in sleep lite mode it is unable to accept any host commands.

The sleep lite feature will allow for any number of LUNs within a selected target to be placed in a low power state through the use of the SET FEATURES by LUN (D5h) command. When multiple LUNs within a target are to remain active the host will need to issue a SET FEATURES by LUN (D5h) command to each LUN that is to be put into sleep lite mode. In the event that the host only wants a single LUN to be active (all other LUNs to be placed into sleep lite mode) two different methods exist. The host could issue SET FEATURES by LUN (D5h) commands to each LUN on the target as suggested in the method 1 example. An alternative solution would be for the host to use a target level SET FEATURES (EFh) command with the sleep lite – Target level enable (P1 = 11b) option as suggested in the method 2 example.

Method 1 for a 2 LUN per CE# configuration example:

1. Issue SET FEATURE by LUN (D5h) command to LUN0 to enable sleep lite (P1 = 01b).
2. LUN0 is in sleep lite mode. LUN2 remains active.

Method 2 for a 2 LUN per CE# configuration example:

1. LUN1 is selected (could be done using READ STATUS ENHANCED (78h) command or other means).
2. Issue SET FEATURE (EFh) command to enable sleep lite – Target level (P1 = 11b)
3. LUN0 enters sleep lite mode. LUN1 remains active.

Because LUNs in sleep lite mode cannot accept host commands the only method for exiting sleep lite mode is by toggling CE#.

Since LUNs in sleep lite cannot accept commands, if GET FEATURE by LUN (D4h) command is issued to a LUN in sleep lite there will be no response. If a GET FEATURE (EEh) command is issued to a target, the target response will only be from the LUNs that are not in sleep lite and the GET FEATURES (EEh) returned data will specify not in sleep lite (P0 = 00h), hence there is no way to check if any of the LUNs on the target are in sleep lite.

Special consideration is taken in the event that on-die termination (ODT) is enabled. If the sleep lite feature is enabled on a LUN that is configured as a target terminator for the selected volume, that LUN should enter the sniff state. This is the same state the LUN enters if it is configured for non-target termination and not on the selected volume. If the LUN is configured as a target terminator for the selected volume and a data burst is occurring, ODT should be enabled regardless of the status of the sleep lite feature. If a LUN is not configured as a target terminator for the selected volume then it should simply enter sleep lite when the sleep lite feature is enabled. See On-die Termination (ODT) section for additional details on ODT functionality.

Table 30: LUN state for Matrix Termination with Sleep Lite Feature

LUN is on Selected Volume?	Terminator for selected Volume?	Sleep Lite Feature Enabled	LUN state
Yes	No	No	Selected
Yes	No	Yes	Sleep lite
Yes	Yes	No	Selected
Yes	Yes	Yes	Sniff
No	Yes	N/A	Sniff
No	No	N/A	Deselected

Volume Select (E1h)

The VOLUME SELECT function is used to select a particular volume based on the address specified. VOLUME SELECT (E1h) command is required to be used when CE# pin reduction is used or when matrix termination is used.

This command is accepted by all targets that share a particular CE# pin. The command may be executed with any LUN on the volume in any state. The VOLUME SELECT (E1h) command may only be issued as the first command after CE# is pulled LOW; CE# shall have remained HIGH for ^{t}CEH and CE# LOW for at least 100ns prior to the command in order for the VOLUME SELECT (E1h) command to be properly received by all NAND targets connected to the host target. The DQS (DQS_t) signal shall remain HIGH for the entire VOLUME SELECT command sequence.

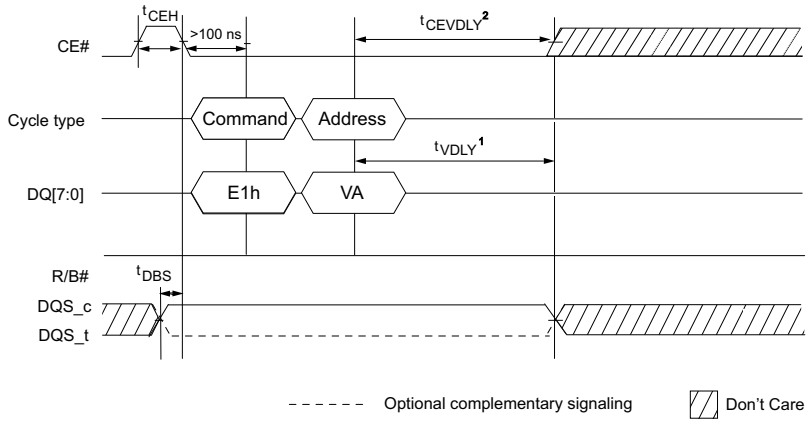
If volumes that share a host target are configured to use different data interfaces, then the host shall issue the VOLUME SELECT (E1h) command using the asynchronous data interface.

When the VOLUME SELECT (E1h) command is issued, all NAND targets that have a volume address that does not match the address specified shall be deselected to save power (equivalent behavior to CE# pulled HGH). If one of the LUNs in an unselected volume is the assigned terminator for the volume addressed, then that LUN will enter the sniff state.

If the volume address specified does not correspond to any appointed volume address, then all NAND targets shall be deselected until a subsequent VOLUME SELECT (E1h) command is issued. If the VOLUME SELECT (E1h) command is not the first command issued after CE# is pulled LOW, then the NAND targets revert to their previous selected, deselected, or sniff states.

The volume address is retained across RESET (FAh, FCh, FFh) commands. A HARD RESET (FDh) command will not undo any previously set volume addressing assignments that were performed prior to the HARD RESET (FDh) command. After HARD RESET (FDh) command is issued the NAND targets do not revert to their previous selected, deselected, or sniff states and a VOLUME SELECT command (E1h) is required to select the desired volume.

Figure 55: VOLUME SELECT (E1h) Operation



Notes: 1. The host shall not issue new commands to any LUN on any volume until after ^{t}VDLY. This delay is required to ensure the appropriate volume is selected for the next command issued. During a data input operation, VOLUME SELECT command may be issued prior to the 10h, 11h, or 15h command if the next command to the volume in data input mode is

change row address. In this case, the host shall wait ^{t}CCS before issuing the CHANGE ROW ADDRESS command.

2. The host shall not bring CE# high on any volume until after ^{t}CEVDLY. This delay is required to ensure the appropriate volume is selected based on the previously issued VOLUME SELECT command.

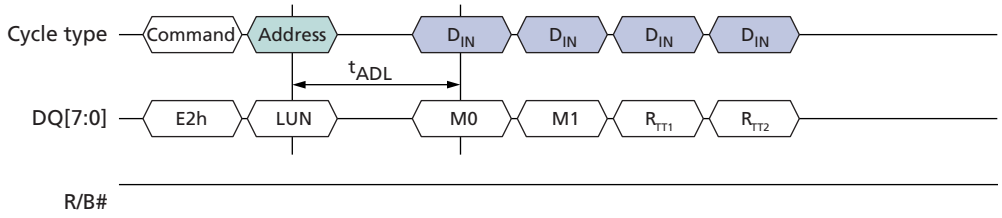
Table 31: Volume Address

	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Volume Address											
VA						Volume Address				-	
Reserved		0	0	0	0					-	

ODT CONFIGURE (E2h)

The ODT CONFIGURE (E2h) command is used to configure on-die termination. Specifically, ODT CONFIGURE (E2h) specifies whether a particular LUN is a terminator for a Volume(s) and the R_{TT} settings. If the LUN is specified as a terminator for one or more Volumes, then the LUN shall enable on-die termination when either data input or data output cycles are executed on the Volume(s) it is acting as a terminator for depending on the settings of Table 32. The on-die termination settings are retained across all RESET (FAh, FCh, FFh) commands.

Figure 56: ODT CONFIGURE (E2h) Operation



The LUN address correspond to the same structure as the last address cycle for the NAND device which determines which LUN will act as the terminator.

The ODT Configuration Matrix structure is defined in Table 32. For the Volume Address fields M0 and M1, if a bit is set to one then the LUN shall act as the terminator for the corresponding Volume(s) (Vn) where n corresponds to the Volume address.

The ODT CONFIGURE (E2h) command is only available while in the NV-DDR2 or NV-DDR3 interface.

If host issues ODT CONFIGURE (E2h) command during a program data load sequence, first the data load sequence must be closed and internal pipeline flushed with an 11h command prior to issuing the command.

Table 32: ODT Configuration Matrix

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value
M0										
Volume Address	Volumes that will be terminated by selected LUN	V7	V6	V5	V4	V3	V2	V1	V0	-
M1										
Volume Address	Volumes that will be terminated by selected LUN	V15	V14	V13	V12	V11	V10	V9	V8	-
R_{TT1}										
DQ[7:0]/DQS_t/DQS_c R_{TT} and ODT enable for data input	ODT disabled (default)					0	0	0	0	0h
	ODT enabled with R_{TT} of 150 Ohms					0	0	0	1	1h
	ODT enabled with R_{TT} of 100 Ohms					0	0	1	0	2h
	ODT enabled with R_{TT} of 75 Ohms					0	0	1	1	3h
	ODT enabled with R_{TT} of 50 Ohms					0	1	0	0	4h
Reserved						0	1	0	1	5h
						0	1	1	0	6h
						0	1	1	1	7h
						1	X	X	X	8h-Fh
DQ[7:0]/DQS_t/DQS_c R_{TT} and ODT enable for data output	ODT disabled (default)	0	0	0	0					0h
	ODT enabled with R_{TT} of 150 Ohms	0	0	0	1					1h
	ODT enabled with R_{TT} of 100 Ohms	0	0	1	0					2h
	ODT enabled with R_{TT} of 75 Ohms	0	0	1	1					3h
	ODT enabled with R_{TT} of 50 Ohms	0	1	0	0					4h
Reserved		0	1	0	1					5h
		0	1	1	0					6h
		0	1	1	1					7h
		1	X	X	X					8h-Fh
R_{TT2}										
RE_t and RE_c R_{TT} ODT enable	ODT disabled (default)					0	0	0	0	0h
	ODT enabled with R_{TT} of 150 Ohms					0	0	0	1	1h
	ODT enabled with R_{TT} of 100 Ohms					0	0	1	0	2h
	ODT enabled with R_{TT} of 75 Ohms					0	0	1	1	3h
	ODT enabled with R_{TT} of 50 Ohms					0	1	0	0	4h

Table 32: ODT Configuration Matrix

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value
Reserved	–					0	1	0	1	5h
						0	1	1	0	6h
						0	1	1	1	7h
						1	X	X	X	8h-Fh
Reserved	–	0	0	0	0					0h

Status Operations

Each LUN provides its status independently of other LUNs on the same target through its 8-bit status register.

After the READ STATUS (70h) or READ STATUS ENHANCED (78h) command is issued, status register output is enabled. The contents of the status register are returned on DQ[7:0] for each data output request.

When the asynchronous or NV-DDR2 interfaces are active and status register output is enabled, changes in the status register are seen on DQ[7:0] as long as CE# and RE# are LOW; it is not necessary to toggle RE# to see the status register update.

When the NV-DDR interface is active and status register output is enabled, changes in the status register are seen on DQ[7:0] as long as CE# and W/R# are LOW and ALE and CLE are HIGH. DQS also toggles (with ^{t}DQSCK delay) while ALE and CLE are captured HIGH. If status register output is enabled and CE# and W/R# are LOW and ALE and CLE are also captured LOW, changes in the status register are still seen asynchronously on DQ[7:0] but DQS does not toggle.

While monitoring the status register to determine when a data transfer from the Flash array to the data register (^{t}R) is complete, the host must issue the READ MODE (00h) command to disable the status register and enable data output (see READ MODE (00h)).

The READ STATUS (70h) command returns the status of the most recently selected LUN. To prevent data contention during or following a multi-LUN operation, the host must enable only one LUN for status output by using the READ STATUS ENHANCED (78h) command (see Interleaved Die (Multi-LUN) Operations).

Table 33: Status Register Definition

SR Bit	Definition	Independent per Plane[1]	Description
7	WP#	–	Write Protect: 0 = Protected 1 = Not protected In the normal array mode, this bit indicates the value of the WP# signal. In OTP mode this bit is set to 0 if a PROGRAM OTP PAGE operation is attempted and the OTP area is protected.
6	RDY	–	Ready/Busy I/O: 0 = Busy 1 = Ready This bit indicates that the selected die (LUN) is not available to accept new commands, address, or data I/O cycles with the exception of RESET LUN (FAh), SYNCHRONOUS RESET (FCh), RESET (FFh), READ STATUS (70h), READ STATUS ENHANCED (78h), and FIXED ADDRESS READ STATUS ENHANCED (71h). This bit applies only to the selected die (LUN).
5	ARDY	–	Ready/Busy Array: 0 = Busy 1 = Ready This bit goes LOW (busy) when an array operation is occurring on any plane of the selected die (LUN). It goes HIGH when all array operations on the selected die (LUN) finish. This bit applies only to the selected die (LUN).
4	–	–	Reserved (0)
3	–	–	Reserved (0)

Table 33: Status Register Definition (Continued)

SR Bit	Definition	Independent per Plane[1]	Description
2	SUSPEND	–	Erase and program suspend: Used in conjunction with FAIL of the status register (SR[0]) SUSPEND = 0, FAIL = 0: ERASE or PROGRAM operation completed with successful status. SUSPEND = 0, FAIL = 1: ERASE or PROGRAM operation completed with fail status. SUSPEND = 1, FAIL = X: ERASE or PROGRAM operation successful suspended FAILC is valid in suspend state (SUSPEND = 1) and provides fail status for previous program immediately completed prior to suspended PROGRAM operation. FAIL is invalid in suspend state (SUSPEND = 1) FAILC is invalid for operations performed after suspend is issued or for the resumed array operation from suspend state.
1	FAILC	Yes	Pass/Fail (N-1): 0 = Pass 1 = Fail This bit is set if the previous PROGRAM operation on the selected die (LUN) failed. This bit is valid only when RDY (SR bit 6) is 1. The valid operations for this bit are PROGRAM-, and COPYBACK PROGRAM-series operations (80h-10h, 80h-15h, 85h-10h). This bit is not valid following an ERASE-series or READ-series operation. This bit is not an indicator for the status of ERASE- or READ-series operations and is not updated even if the previous operation was a program command. This bit retains the status of the previous valid PROGRAM operation when the most recent PROGRAM operation is complete. For example, if an ERASE or READ operation is complete and the previous operation was a PROGRAM operation the FAILC bit will not provide pass/fail status information for the previous PROGRAM operation. The FAILC bit will only provide pass/fail status information if the most recently finished operation was a PROGRAM operation.
0	FAIL	Yes	Pass/Fail (N): 0 = Pass 1 = Fail This bit is set if the most recently finished operation on the selected die (LUN) failed. This bit is valid only when ARDY (SR bit 5) is 1. It applies to PROGRAM-, ERASE-, and COPYBACK PROGRAM-series operations (80h-10h, 80h-15h, 60h-D0h, 85h-10h). This bit is not valid following a READ-series operation.

Notes: 1. After a multi-plane operation begins, the FAILC and FAIL bits are ORed together for the active planes when the READ STATUS (70h) command or FIXED ADDRESS READ STATUS ENHANCED (71h) command are issued. After the READ STATUS ENHANCED (78h) command is issued, the FAILC and FAIL bits reflect the status of the plane selected.

2. In addition to WP# status, SR[7] also provides LOCK Status (SR[7] = 0) to indicate the host issued a command that was blocked from execution by the NAND. The LOCK Status is cleared upon the host issuing the next valid array operation command. The LOCK Status is Plane independent. If the user issues READ STATUS ENHANCED (78h) or FIXED ADDRESS READ STATUS ENHANCED (71h) to a non-active plane (planes not enabled by user are deemed non-active), then LOCK status (SR[7]) will be invalid.

READ STATUS (70h)

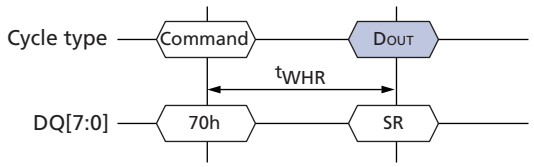
The READ STATUS (70h) command returns the status of the last-selected die (LUN) on a target. This command is accepted by the last-selected die (LUN) even when it is busy (RDY = 0).

If there is only one die (LUN) per target, the READ STATUS (70h) command can be used to return status following any NAND command.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select the die (LUN) that should report status. In this situation, using the READ STATUS (70h) command will result in bus contention, as two or more die (LUNs) could respond until the next operation is issued. The READ STATUS (70h) command can be used following all single die (LUN) operations.

If following a multi-plane operation, regardless of the number of LUNs per target, the READ STATUS (70h) command indicates an error occurred (FAIL = 1), use the READ STATUS ENHANCED (78h) command—once for each plane—to determine which plane operation failed.

Figure 57: READ STATUS (70h) Operation



READ STATUS ENHANCED (78h)

The READ STATUS ENHANCED (78h) command returns the status of the addressed die (LUN) on a target even when it is busy (RDY = 0). This command is accepted by all die (LUNs), even when they are BUSY (RDY = 0).

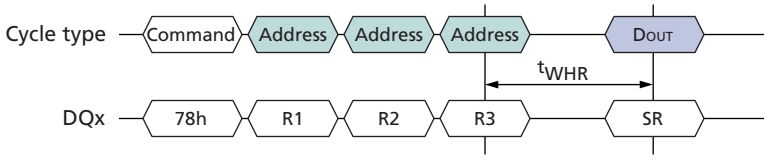
Writing 78h to the command register, followed by three row address cycles containing the page, block, and LUN addresses, puts the selected die (LUN) into read status mode. The selected die (LUN) stays in this mode until another valid command is issued. Die (LUNs) that are not addressed are deselected to avoid bus contention.

The selected LUN's status is returned when the host requests data output. The RDY and ARDY bits of the status register are shared for all of the planes of the selected die (LUN). The FAILC and FAIL bits are specific to the plane specified in the row address.

The READ STATUS ENHANCED (78h) command also enables the selected die (LUN) for data output. To begin data output following a READ-series operation after the selected die (LUN) is ready (RDY = 1), issue the READ MODE (00h) command, then begin data output. If the host needs to change the cache register that will output data, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command after the die (LUN) is ready (see CHANGE READ COLUMN ENHANCED (06h-E0h)).

Use of the READ STATUS ENHANCED (78h) command is prohibited during the power-on RESET (FFh) command and when OTP mode is enabled. It is also prohibited following some of the other RESET, identification, and configuration operations. See individual operations for specific details.

Figure 58: READ STATUS ENHANCED (78h) Operation



FIXED ADDRESS READ STATUS ENHANCED (71h)

The FIXED ADDRESS READ STATUS ENHANCED (71h) command returns the status of the addressed die (LUN) on a target even when it is busy (RDY = 0). This command is accepted by all die (LUNs), even when they are BUSY (RDY = 0). The FIXED ADDRESS READ STATUS ENHANCED (71h) command can be used instead of READ STATUS ENHANCED (78h) command, but address cycle bit locations are fixed and do not change based on NAND architecture, number of bits per cell, or any mode selections.

Use of the FIXED ADDRESS READ STATUS ENHANCED (71h) command is allowed during the power-on RESET (FFh) command (during ^{t}POR) and when OTP mode is enabled. It is also allowed following some of the other RESET, IDENTIFICATION, and CONFIGURATION operations that READ STATUS ENHANCED (78h) is prohibited.

Writing 71h to the command register, followed by one row address cycle containing the hardcoded LUN selections, puts the selected die (LUN) into read status mode. The selected die (LUN) stays in this mode until another valid command is issued. Die (LUNs) that are not addressed are deselected to avoid bus contention.

The status output for FIXED ADDRESS READ STATUS ENHANCED (71h) command is identical to the status output for READ STATUS ENHANCED (78h) command. The selected LUN's status is returned when the host requests data output. The RDY, ARDY, FAILC, and FAIL bits of the status register are shared for all of the planes of the selected die (LUN).

The FIXED ADDRESS READ STATUS ENHANCED (71h) command also enables the selected die (LUN) for data output. To begin data output following a READ-series operation after the selected die (LUN) is ready (RDY = 1), issue the READ MODE (00h) command, then begin data output. If the host needs to change the cache register that will output data, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command after the die (LUN) is ready (see CHANGE READ COLUMN ENHANCED (06h-E0h)).

Figure 59: FIXED ADDRESS READ STATUS ENHANCED (71h) Operation

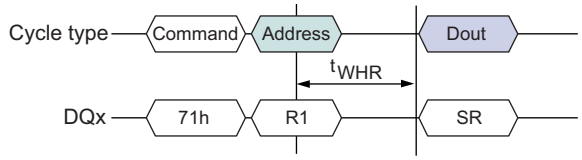


Table 34: R1 Address Cycle Decoding for FIXED ADDRESS READ STATUS ENHANCED (71h) Operation

Description	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
R1											
Bit LA0 (DQ0) for LUN selection	LUN0								0	0b	
	LUN1								1	1b	
Reserved	Don't Care	–	–	–	–	–	–	–			1

Note: 1. Must be "0".

Column Address Operations

The column address operations affect how data is input to and output from the cache registers within the selected die (LUNs). These features provide host flexibility for managing data, especially when the host internal buffer is smaller than the number of data bytes or words in the cache register.

When the asynchronous interface is active, column address operations can address any byte in the selected cache register.

When the synchronous interface is active, column address operations are aligned to word boundaries (CA0 is forced to 0), because as data is transferred on DQ[7:0] in two-byte units.

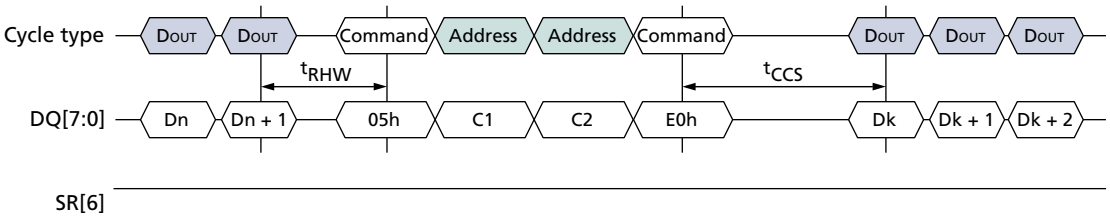
CHANGE READ COLUMN (05h-E0h)

The CHANGE READ COLUMN (05h-E0h) command changes the column address of the selected cache register and enables data output from the last selected die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1).

Writing 05h to the command register, followed by two column address cycles containing the column address, followed by the E0h command, puts the selected die (LUN) into data output mode. After the E0h command cycle is issued, the host must wait at least ^{t}CCS before requesting data output. The selected die (LUN) stays in data output mode until another valid command is issued.

In devices with more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be issued prior to issuing the CHANGE READ COLUMN (05h-E0h). In this situation, using the CHANGE READ COLUMN (05h-E0h) command without the READ STATUS ENHANCED (78h) command will result in bus contention, as two or more die (LUNs) could output data.

Figure 60: CHANGE READ COLUMN (05h–E0h) Operation



CHANGE READ COLUMN ENHANCED (06h-E0h)

The CHANGE READ COLUMN ENHANCED (06h-E0h) command enables data output on the addressed die's (LUN's) cache register at the specified column address. This command is accepted by a die (LUN) when it is ready (RDY = 1; ARDY = 1).

Writing 06h to the command register, followed by two column address cycles and three row address cycles, followed by E0h, enables data output mode on the address LUN's cache register at the specified column address. Only the column, plane and LUN addresses are valid; the page and block addresses are ignored. After the E0h command cycle is issued, the host must wait at least ^{t}CCS before requesting data output. The selected die (LUN) stays in data output mode until another valid command is issued.

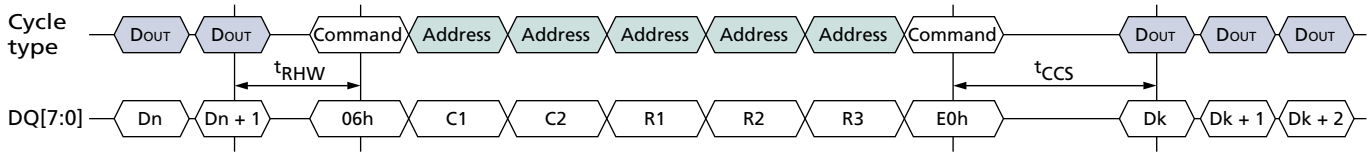
Following a MULTI-PLANE READ PAGE operation, the CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to select the cache register to be enabled for data output. After data output is complete on the selected plane, the command can be issued again to begin data output on another plane.

In devices with more than one die (LUN) per target, after all of the die (LUNs) on the target are ready (RDY = 1), the CHANGE READ COLUMN ENHANCED (06h-E0h) command can be used following an interleaved die (multi-LUN) READ operation. Die (LUNs) that are not addressed are deselected to avoid bus contention.

In devices with more than one die (LUN) per target, during interleaved die (multi-LUN) operations where more than one or more die (LUNs) are busy (RDY = 1; ARDY = 0 or RDY = 0; ARDY = 0), the READ STATUS ENHANCED (78h) command must be issued to the die (LUN) to be selected prior to issuing the CHANGE READ COLUMN ENHANCED (06h-E0h). In this situation, using the CHANGE READ COLUMN ENHANCED (06h-E0h) command without the READ STATUS ENHANCED (78h) command will result in bus contention, as two or more die (LUNs) could output data.

If there is a need to update the column address without selecting a new cache register or LUN, the CHANGE READ COLUMN (05h-E0h) command can be used instead.

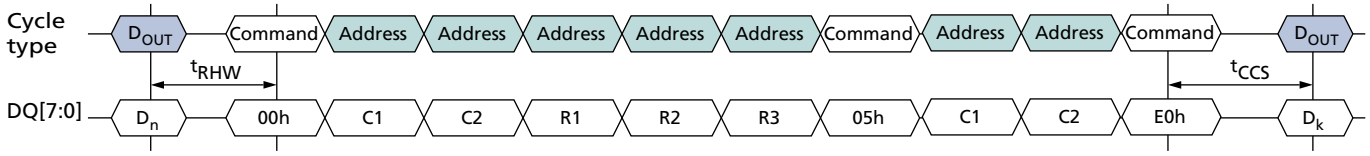
Figure 61: CHANGE READ COLUMN ENHANCED (06h–E0h) Operation



CHANGE READ COLUMN ENHANCED (00h-05h-E0h)

This operation behaves the same as the CHANGE READ COLUMN ENHANCED (06h-E0h) command.

Figure 62: CHANGE READ COLUMN ENHANCED (00h-05h-E0h) Operation



CHANGE WRITE COLUMN (85h)

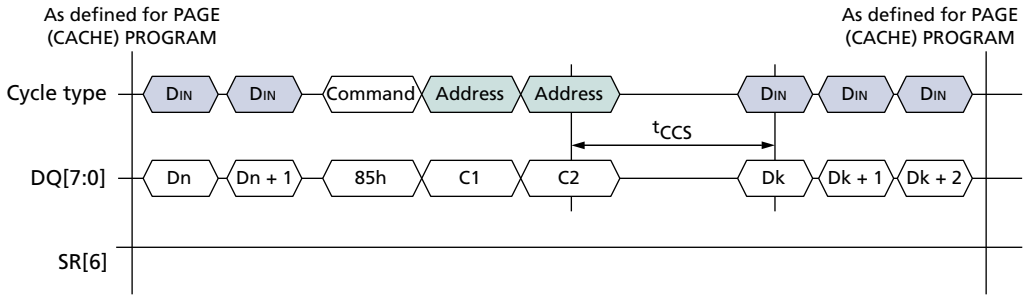
The CHANGE WRITE COLUMN (85h) command changes the column address of the selected cache register and enables data input on the last-selected die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during cache program operations (RDY = 1; ARDY = 0).

Writing 85h to the command register, followed by two column address cycles containing the column address, puts the selected die (LUN) into data input mode. After the second address cycle is issued, the host must wait at least ^{t}CCS before inputting data. The selected die (LUN) stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The CHANGE WRITE COLUMN (85h) command is allowed after the required address cycles are specified, but prior to the final command cycle (10h, 11h, 15h) of the following commands while data input is permitted: PROGRAM PAGE (80h-10h), PROGRAM PAGE MULTI-PLANE (80h-11h), PROGRAM PAGE CACHE (80h-15h), COPYBACK PROGRAM (85h-10h), and COPYBACK PROGRAM MULTI-PLANE (85h-11h).

In devices that have more than one die (LUN) per target, the CHANGE WRITE COLUMN (85h) command can be used with other commands that support interleaved die (multi-LUN) operations.

Figure 63: CHANGE WRITE COLUMN (85h) Operation



CHANGE ROW ADDRESS (85h)

The CHANGE ROW ADDRESS (85h) command changes the row address (block and page) where the cache register contents will be programmed in the NAND Flash array. It also changes the column address of the selected cache register and enables data input on the specified die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during CACHE PROGRAMMING operations (RDY = 1; ARDY = 0).

Write 85h to the command register. Then write two column address cycles and three row address cycles. This updates the page and block destination of the selected plane for the addressed LUN and puts the cache register into data input mode. After the fifth address cycle is issued the host must wait at least ^{t}CCS before inputting data. The selected LUN stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The CHANGE ROW ADDRESS (85h) command is allowed after the required address cycles are specified, but prior to the final command cycle (10h, 11h, 15h) of the following commands while data input is permitted: PROGRAM PAGE (80h-10h), PROGRAM PAGE MULTI-PLANE (80h-11h), PROGRAM PAGE CACHE (80h-15h), COPYBACK PROGRAM (85h-10h), and COPYBACK PROGRAM MULTI-PLANE (85h-11h). When used with these commands, the LUN address and plane select bits are required to be identical to the LUN address and plane select bits originally specified.

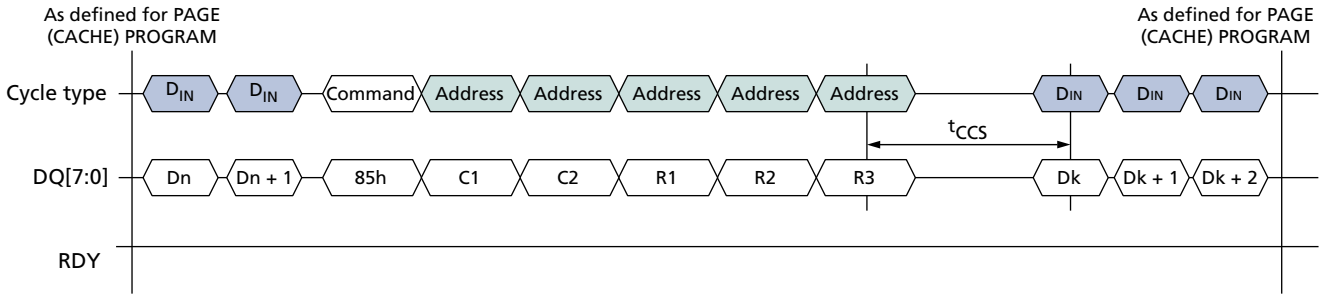
The CHANGE ROW ADDRESS (85h) command enables the host to modify the original page and block address for the data in the cache register to a new page and block address.

In devices that have more than one die (LUN) per target, the CHANGE ROW ADDRESS (85h) command can be used with other commands that support interleaved die (multi-LUN) operations.

The CHANGE ROW ADDRESS (85h) command can be used with the CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h) commands to read and modify cache register contents in small sections prior to programming cache register contents to the NAND Flash array. This capability can reduce the amount of buffer memory used in the host controller.

To modify the cache register contents in small sections, first issue a PAGE READ (00h-30h) or COPYBACK READ (00h-35h) operation. When data output is enabled, the host can output a portion of the cache register contents. To modify the cache register contents, issue the 85h command, the column and row addresses, and input the new data. The host can re-enable data output by issuing the 11h command, waiting ^{t}DBSY, and then issuing the CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h) command. It is possible toggle between data output and data input multiple times. After the final CHANGE ROW ADDRESS (85h) operation is complete, issue the 10h command to program the cache register to the NAND Flash array.

Figure 64: CHANGE ROW ADDRESS (85h) Operation



READ Operations

Read operations are used to copy data from the NAND Flash array of one or more of the planes to their respective cache registers and to enable data output from the cache registers to the host through the DQ bus.

Read Operations

The READ PAGE (00h-30h) command, when issued by itself, reads one page from the NAND Flash array to its cache register and enables data output for that cache register.

During data output the following commands can be used to read and modify the data in the cache registers: CHANGE READ COLUMN (05h-E0h) and CHANGE ROW ADDRESS (85h).

Multi-Plane Read Operations

MULTI-PLANE READ PAGE operations improve data throughput by copying data from more than one plane simultaneously to the specified cache registers. This is done by prepending one or more READ PAGE MULTI-PLANE (00h-32h) commands in front of the READ PAGE (00h-30h) command.

When the die (LUN) is ready, the CHANGE READ COLUMN ENHANCED (06h-E0h) command determines which plane outputs data. During data output, the following commands can be used to read and modify the data in the cache registers: CHANGE READ COLUMN (05h-E0h) and CHANGE ROW ADDRESS (85h). See Multi-Plane Operations for details.

See Multi-Plane Operations for additional multi-plane addressing requirements

READ MODE (00h)

The READ MODE (00h) command disables status output and enables data output for the last-selected die (LUN) and cache register after a READ operation (00h-30h, 00h-35h) has been monitored with a status operation (70h, 78h, 71h). This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) prior to issuing the READ MODE (00h) command. This prevents bus contention.

READ PAGE (00h-30h)

The READ PAGE (00h–30h) command copies a page from the NAND Flash array to its respective cache register and enables data output. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

To read a page from the NAND Flash array, write the 00h command to the command register, the write five address cycles to the address registers, and conclude with the 30h command. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}R as data is transferred.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h, 71h) can be used. If the status operations are used to monitor the LUN's status, when the die (LUN) is ready

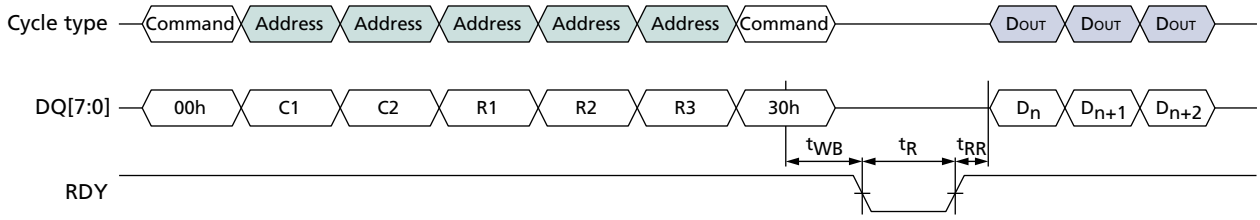
(RDY = 1, ARDY = 1), the host disables status output and enables data output by issuing the READ MODE (00h) command. When the host requests data output, output begins at the column address specified.

During data output the CHANGE READ COLUMN (05h-E0h) command can be issued.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) prior to the issue of the READ MODE (00h) command. This prevents bus contention.

The READ PAGE (00h-30h) command is used as the final command of a MULTI-PLANE READ operation. It is preceded by one or more READ PAGE MULTI-PLANE (00h-32h) commands. Data is transferred from the NAND Flash array for all of the addressed planes to their respective cache registers. When the die (LUN) is ready (RDY = 1, ARDY = 1), data output is enabled for the cache register linked to the least significant plane addressed, regardless of input order. When the host requests data output, output begins at the column address last specified in the READ PAGE (00h-30h) command. The CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to enable data output in the other cache registers. See Multi-Plane Operations for additional multi-plane addressing requirements.

Figure 65: READ PAGE (00h–30h) Operation



READ PAGE MULTI-PLANE (00h–32h)

The READ PAGE MULTI-PLANE (00h-32h) command queues a plane to transfer data from the NAND flash array to its cache register. This command can be issued one or more times. Each time a new plane address is specified, that plane is also queued for data transfer. The READ PAGE (00h-30h) command is issued to select the final plane and to begin the read operation for all previously queued planes. All queued planes will transfer data from the NAND Flash array to their cache registers.

To issue the READ PAGE MULTI-PLANE (00h-32h) command, write 00h to the command register, then write five address cycles to the address register, and conclude by writing 32h to the command register. The column address in the address specified is ignored.

After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}DBSY. After ^{t}DBSY, R/B# goes HIGH and the die (LUN) is ready (RDY = 1, ARDY = 1). At this point, the die (LUN) and block are queued for data transfer from the array to the cache register for the addressed plane. During ^{t}DBSY, the only valid commands are status operations (70h, 78h) and reset commands (FFh, FCh). Following ^{t}DBSY, to continue the MULTI-PLANE READ operation, the only valid commands are status operations (70h, 78h), READ PAGE MULTI-PLANE (00h-32h), and READ PAGE (00h-30h).

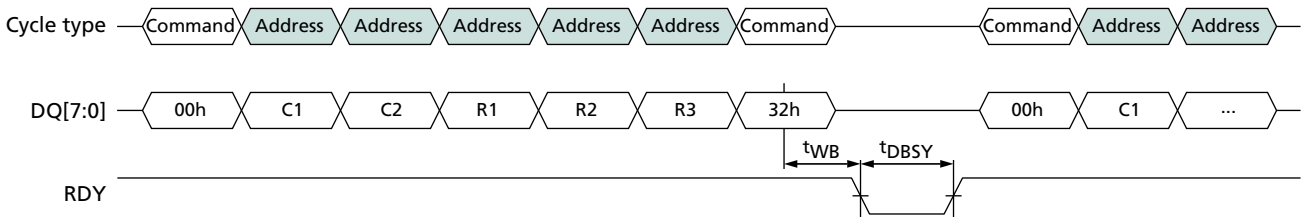
Additional READ PAGE MULTI-PLANE (00h-32h) commands can be issued to queue additional planes for data transfer.

If the READ PAGE (00h-30h) command is used as the final command of a MULTI-PLANE READ operation, data is transferred from the NAND Flash array for all of the addressed planes to their respective cache registers. When the die (LUN) is ready (RDY = 1, ARDY = 1), data output is enabled for the cache register linked to the last even plane addressed. When the host requests data output, it begins at the column address specified in the

READ PAGE (00h-30h) command. To enable data output in the other cache registers, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command. Additionally, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address within the currently selected plane.

See for Multi-Plane Operationsadditional multi-plane addressing requirements.

Figure 66: READ PAGE MULTI-PLANE (00h–32h) Operation



Read Retry Operations

Read Retry Operations are used as an additional method to recover from bit errors beyond the ECC correction threshold.

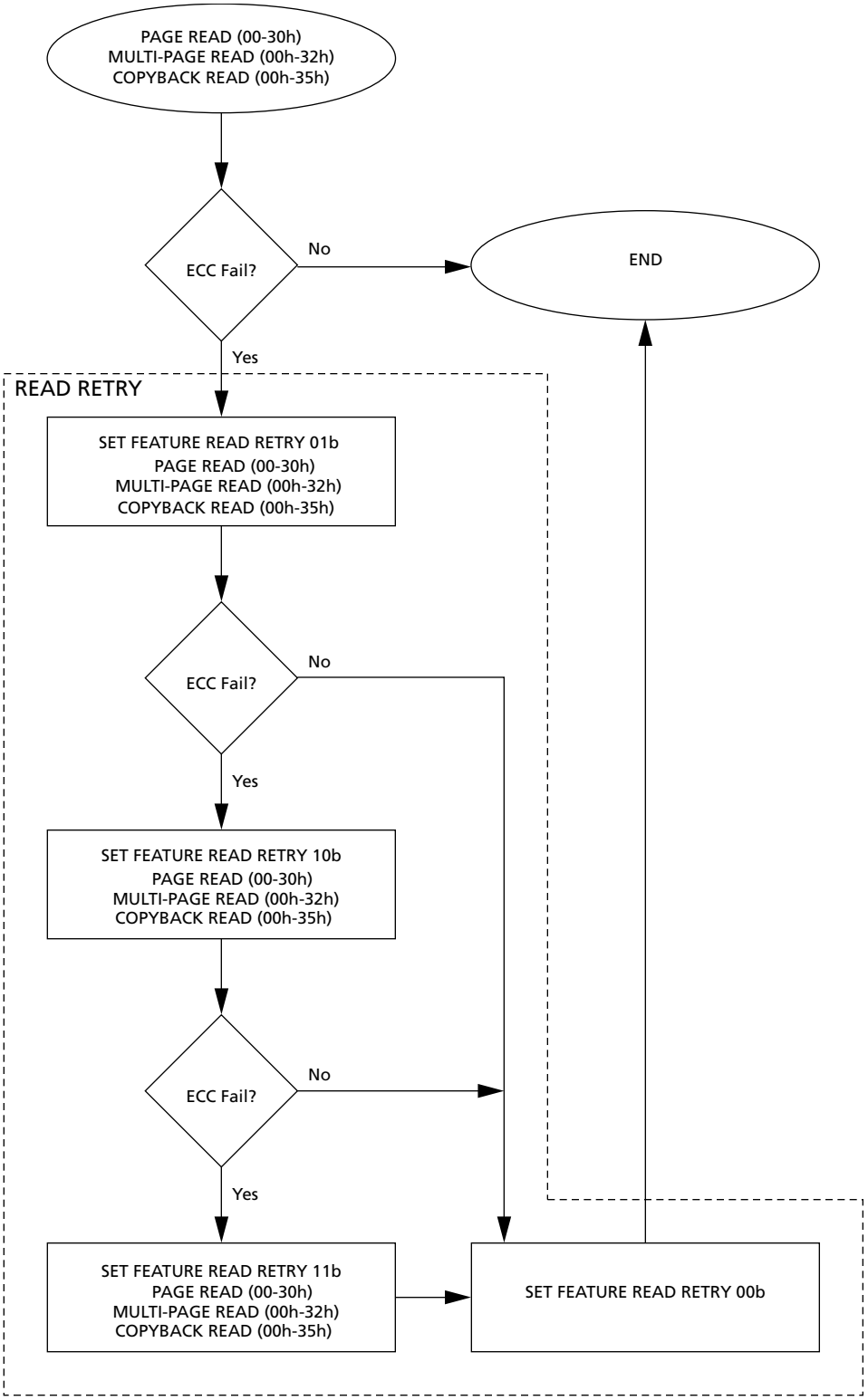
Read Retry Operations

The Read Retry Operations are a coordination of Read Operations and Set Features (EFh) with Feature Address 89h selecting different internal read settings in attempt to recover data that is beyond the ECC correction threshold. Using the Read Retry Operations with any array Read Operation commands is allowed. See Table 23, Feature Addresses 89h: Read Retry for details.

If reading a page has failed for bit errors beyond the ECC correction threshold, the host issues the SET FEATURE (EFh) command to feature address 89h with P1 subfeature set to a Read Retry option as defined in that feature address. A new NAND array Read Operation can now be performed. If the read still fails for bit errors beyond the ECC correction threshold, issue the SET FEATURES (EFh) command with the Read Retry (89h) feature address to select the next consecutive Read Retry option and repeat Read Retry Operations until the data is correctable or the last option has been attempted. If the reread is now correctable within the ECC threshold limits, the next Read Retry option should be set to its default value before the next NAND array Read Operation. See Figure 67 for flow diagram of Read Retry Operations.

When the user writes to the Read Retry feature address then all subsequent reads use the internal NAND settings associated with that value until either the Read Retry feature address is rewritten or the device is powered down. This feature should not be used with the following commands: READ PARAMETER PAGE (ECh), READ UNIQUE ID (EDh), READ OTP PAGE (00h-30h).

Figure 67: Read Retry flow chart



Note: 1. There may be more read retry options than are shown in the figure for this NAND device. See Configuration Operations and Read Retry (89h) feature address for details.

Program Operations - Single Pass Programming

Program operations are used to move data from the cache or data registers to the NAND array of one or more planes. During a PROGRAM operation the contents of the cache and/or data registers are modified by the internal control logic. The MLC single pass programming sequence requires both lower and upper associated shared pages be entered before data is programmed into the array. Lower page data must be entered before the upper page data. After data has been entered to a lower page address, the program confirm command (10h) will trigger the LUN to move the data from the cache register into internal page buffer latches, ^{t}PSBY. After data has been entered to an upper page address, the confirm command (10h) will trigger the LUN to begin the PROGRAM operation.

Within a block, pages must be programmed sequentially from the least significant page address to the most significant page address (for example, 0, 1, 2, 3, …). Programming pages out of order within a block is prohibited.

The PROGRAM PAGE (80h-10h) command is used to enter the lower page address and data into the cache register. After the 10h command is entered the LUN will go busy (RDY = 0, ARDY = 0) for ^{t}PBSY while data is transferred from the cache register into the page buffer latches. A second PROGRAM PAGE (80h-10h) operation is used to enter the upper page address and data into the cache register. After the 10h command is entered the LUN will go busy (RDY = 0, ARDY = 0) for ^{t}PROG while data is written to the array. If RESET (FFh, FCh, FAh) is issued anytime during the program sequence prior to ^{t}PROG time (including ^{t}PBSY time), the program sequence is aborted and must be re-started from the beginning. Data in the page registers is valid.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the READ STATUS (70h, 78h) operations may be used. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the status of the FAIL bit.

It is the responsibility of the host to ensure that the lower page and upper page address are associated shared pages (see Shared Pages section). No internal address checks are performed by the LUN. In the event that the lower page and upper page addresses are not associated shared pages, the data will be programmed to the lower and upper pages specified by the upper page address, and the lower page data will not be valid.

After lower page data has been entered via PROGRAM PAGE (80h-10h) command, if a second PROGRAM PAGE (80h-10h) command is issued with a lower page address to the same plane, the data entered into the first lower page address will be overwritten. A subsequent (80h-10h) command sequence with upper page address and data will still be required to trigger the start of the program algorithm.

Use of READ PAGE (00h-30h) and READ PAGE MULTI-PLANE (00h-32h) commands are allowed to be performed in between lower page and upper page data entry to other pages and/or LUNs. ERASE operations using ERASE BLOCK (60h-D0h) commands are also allowed in between lower page and upper page data entry as long as the ERASE operation does not occur in the same plane and same LUN as the SINGLE PASS PROGRAMMING operation.

While in a single pass programming sequence, all Cache read operations (00h-31h, 31h, 3Fh) are prohibited between lower page and upper page data entry. READ RETRY operations that invoke a longer ^{t}R time (see Configuration Operations section, feature address 89h: read retry for details) are also prohibited between lower page and upper page data entry. Programming operations to other blocks on the same die (LUN) are prohibited between lower page and upper page data entry.

PROGRAM SUSPEND (84h) AND PROGRAM RESUME (13h) operations are supported within a single pass programming sequence. See Program Suspend (84h) and Program Resume (13h) for description of the use of suspend and resume operations.

Pages that are mapped without a shared page require only a single PROGRAM PAGE (80h-10h) operation. See Shared Pages section for details.

The PROGRAM PAGE MULTI-PLANE (80h-11h) command can also be used with single pass programming. Special care must be taken to ensure the command sequence follows the correct order when multi-plane programming operations are being used. Because the LUN is triggered to move data from the cache register into the internal page buffer latches only after the confirm command (10h) associated with data loaded to a lower page address, data must first be loaded into the lower page of each plane before upper page data can be loaded. Multi-Plane operations follow all of the same restrictions as single-plane operations.

The following are examples of program command sequences using the single pass programming sequence.

Example command sequence for PROGRAM PAGE (80h-10h) with single pass programming for one plane:

1. Issue PROGRAM PAGE (80h-10h) with lower page data
2. Wait ^{t}PBSY
3. Issue PROGRAM PAGE (80h-10h) with upper page data
4. Wait ^{t}PROG

Example command sequence for PROGRAM PAGE MULTI-PLANE (80h-11h) with single pass programming for two planes:

1. Issue PROGRAM PAGE MULTI-PLANE (80h-11h) with Plane 0 lower page data
2. Issue PROGRAM PAGE (80h-10h) with Plane 1 lower page data
3. Wait ^{t}PBSY
4. Issue PROGRAM PAGE MULTI-PLANE (80h-11h) with Plane 0 upper page data
5. Issue PROGRAM PAGE (80h-10h) with Plane 1 upper page data
6. Wait ^{t}PROG

Example command sequence for COPYBACK PROGRAM (85h-10h) with single pass programming for one plane:

1. Issue COPYBACK READ (00h-35h). It is possible for the COPYBACK READ (00h-35h) command to address a different block or page type from the subsequent 85h command, however both the 00h-35h and 85h commands must address the same plane.
2. Read data out and identify errors
3. Issue CHANGE WRITE COLUMN (85h) + 5 address cycles (addressed to a lower page) to address of first error and enter corrected data. Repeat error correction by issuing CHANGE WRITE COLUMN (85h) + 2 column address cycles until all errors are corrected, then issue 10h command.
4. Wait ^{t}PBSY
5. Issue COPYBACK READ (00h-35h) to another address
6. Read data out and identify errors
7. Issue CHANGE WRITE COLUMN (85h) + 5 address cycles (addressed to an upper page) to address of first error and enter corrected data. Repeat error correction by issuing CHANGE WRITE COLUMN (85h) + 2 column address cycles until all errors are corrected, then issue 10h command.
8. Wait ^{t}PROG

Example command sequence for MULTI-PLANE PROGRAM with READ PAGE Interrupt with single pass programming with two planes:

1. Issue PROGRAM PAGE MULTI-PLANE (80h-11h) with Plane 0 lower page data
2. Issue PROGRAM PAGE (80h-10h) with Plane 1 lower page data
3. Wait ^{t}PBSY
4. Issue PROGRAM PAGE MULTI-PLANE (80h-11h) with Plane 0 upper page data
5. Issue PROGRAM PAGE (80h-10h) with Plane 1 upper page data
6. After ^{t}PROG has started but has not yet finished, Issue PROGRAM SUSPEND (84h) with 5 cycle address
7. Wait ^{t}PSPD
8. Issue READ PAGE MULTI-PLANE (00h-32h) to Plane 0
9. Issue READ PAGE (00h-30h) to Plane 1
10. Wait ^{t}R
11. Read out data from Plane 0 and Plane 1
12. Issue PROGRAM RESUME (13h) with 5 cycle address
13. Wait ^{t}PROG

Figure 68: PROGRAM PAGE (80h-10h) Operation with Single Pass Programming

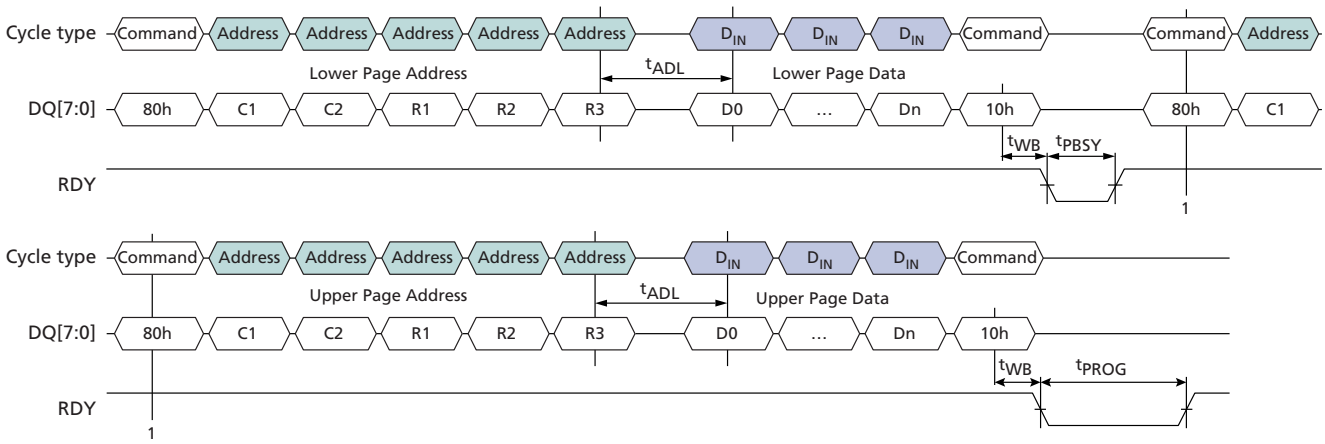
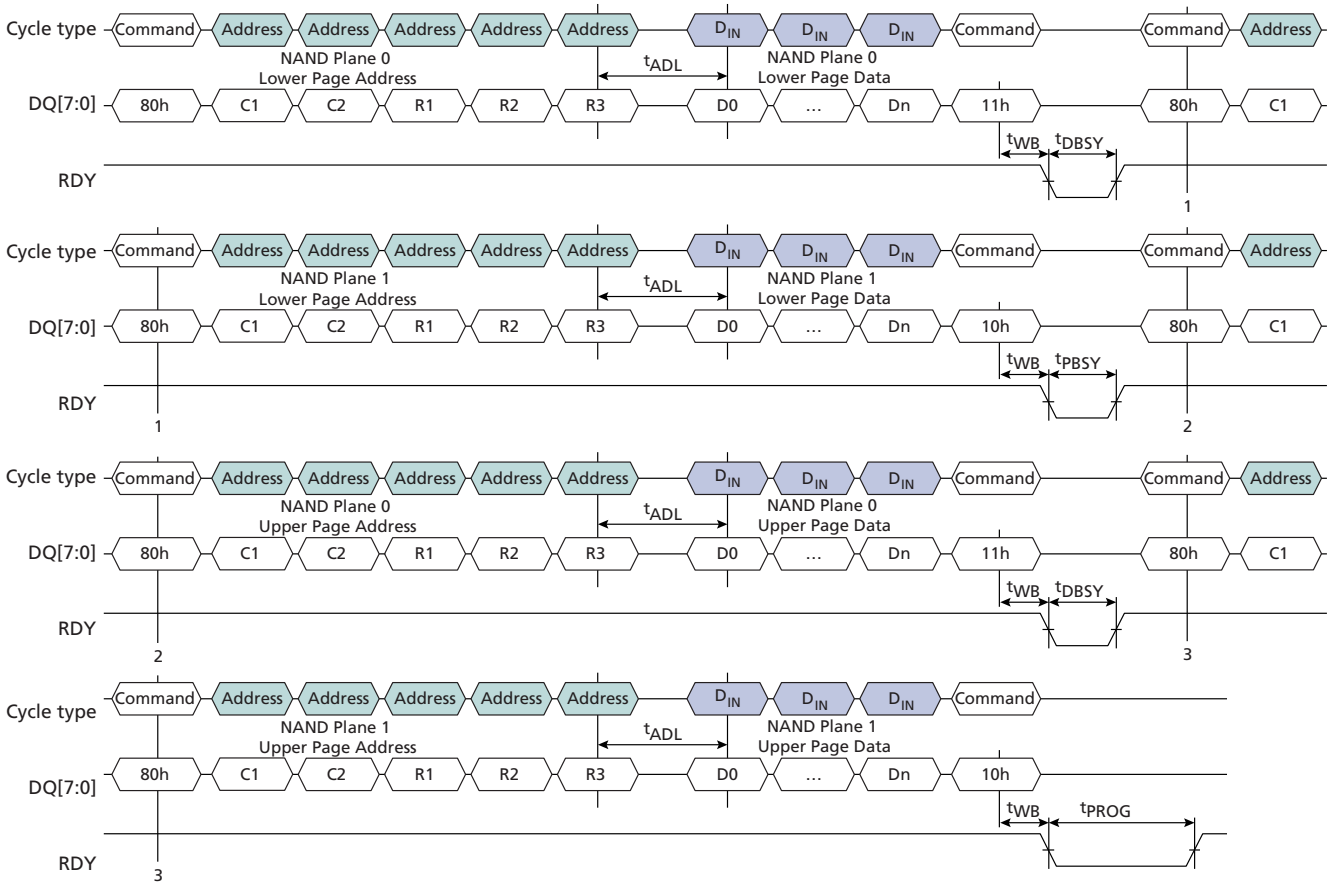


Figure 69: PROGRAM PAGE MULTI-PLANE (80h-11h) Operation with Single Pass Programming



Program Operations

The PROGRAM PAGE (80h-10h) command, when not preceded by the PROGRAM PAGE MULTI-PLANE (80h-11h) command, programs one page from the cache register to the NAND Flash array. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that the operation has completed successfully.

Multi-Plane Program Operations

The PROGRAM PAGE MULTI-PLANE (80h-11h) command can be used to improve PROGRAM operation system performance by enabling multiple pages to be moved from the cache registers to different planes of the NAND Flash array. This is done by prepending one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands in front of the PROGRAM PAGE (80h-10h) command. See Multi-Plane Operations for details.

PROGRAM PAGE (80h-10h)

The PROGRAM PAGE (80h-10h) command enables the host to input data to a cache register, and move the data from the cache register to the specified block and page address in the array of the selected die (LUN). This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

To input a page to the cache register and move it to the NAND array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by a PROGRAM PAGE MULTI-PLANE (80h-11h) command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Then write five address cycles containing the column address and row address of the lower page address. Data input cycles follow for the lower page address. Serial data is input beginning at the column address specified. At any time during the data input cycle the CHANGE WRITE COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands may be issued. When data input is complete, write 10h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for ^{t}PBSY as the lower page data is transferred.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) may be used. When the die (LUN) is ready (RDY = 1, ARDY = 1).

After the lower page data is committed, write another 80h to the command register. Then write five address cycles containing the column address and row address of the upper page address. Data input cycles follow for the upper page address. Serial data is input beginning at the column address specified. At any time during the data input cycle the CHANGE WRITE COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands may be issued. When data input is complete, write 10h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for ^{t}PROG as both the lower page data and upper page data is programmed.

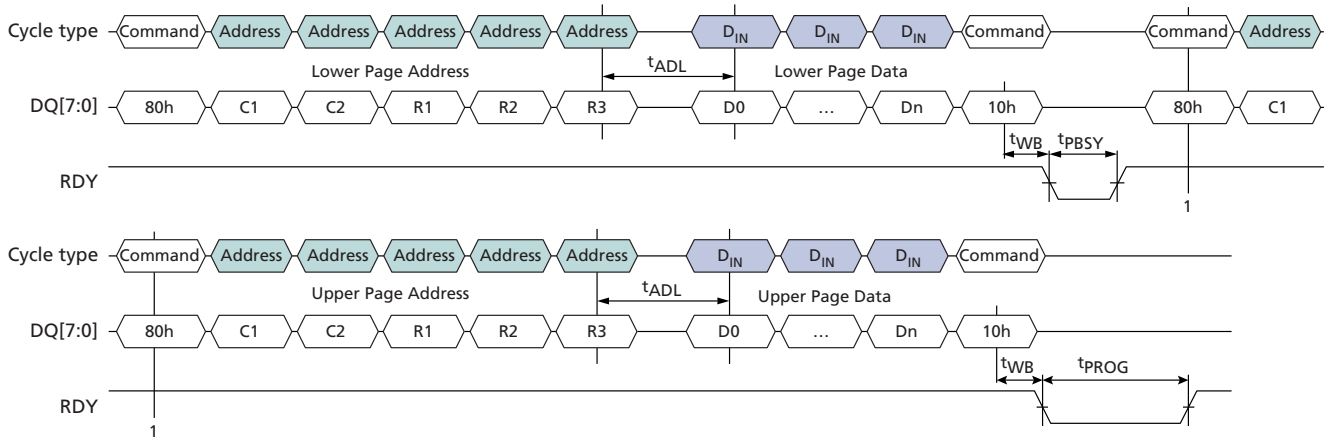
To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) may be used. When the die (LUN) is ready (RDY = 1, ARDY = 1).

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

When the last PROGRAM PAGE (80h-10h) command is used as the final command of a MULTI-PLANE PROGRAM operation, it is preceded by one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands, data is transferred from the cache registers for all of the addressed planes to the NAND array. The host should check the status of the operation by using the status operations (70h, 78h).

See Multi-Plane Addressing for multi-plane addressing requirements.

Figure 70: PROGRAM PAGE (80h–10h) Operation



PROGRAM PAGE MULTI-PLANE (80h-11h)

The PROGRAM PAGE MULTI-PLANE (80h-11h) command enables the host to input data to the addressed plane's cache register and queue the cache register to ultimately be moved to the NAND Flash array. This command can be issued one or more times. Each time a new plane address is specified that plane is also queued for data transfer. To input data for the final plane and to begin the PROGRAM operation for all previously queued planes, issue the PROGRAM PAGE (80h-10h) command. All of the queued planes will move the data to the NAND Flash array. This command is accepted by the die (LUN) when it is ready (RDY = 1).

To input a page to the cache register and queue it to be moved to the NAND Flash array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by an 11h command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Write five address cycles containing the column address and row address for a lower page; data input cycles follow for the lower page. Serial data is input beginning at the column address specified. At any time during the data input cycle, the CHANGE WRITE COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands can be issued. When data input is complete, write 11h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}DBSY.

To determine the progress of ^{t}DBSY, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) can be used.

When the LUN's status shows that it is ready (RDY = 1) and the lower page data is committed for the first NAND plane enter, write another 80h to the command register and then write five address cycles containing the column address and row address of the lower page address of another NAND plane. Data input cycles follow for the lower page address of the NAND plane. Serial data is input beginning at the column address specified. At any time during the data input cycle the CHANGE WRITE COLUMN (85h) and

CHANGE ROW ADDRESS (85h) commands may be issued. When data input is complete, write 11h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}DBSY.

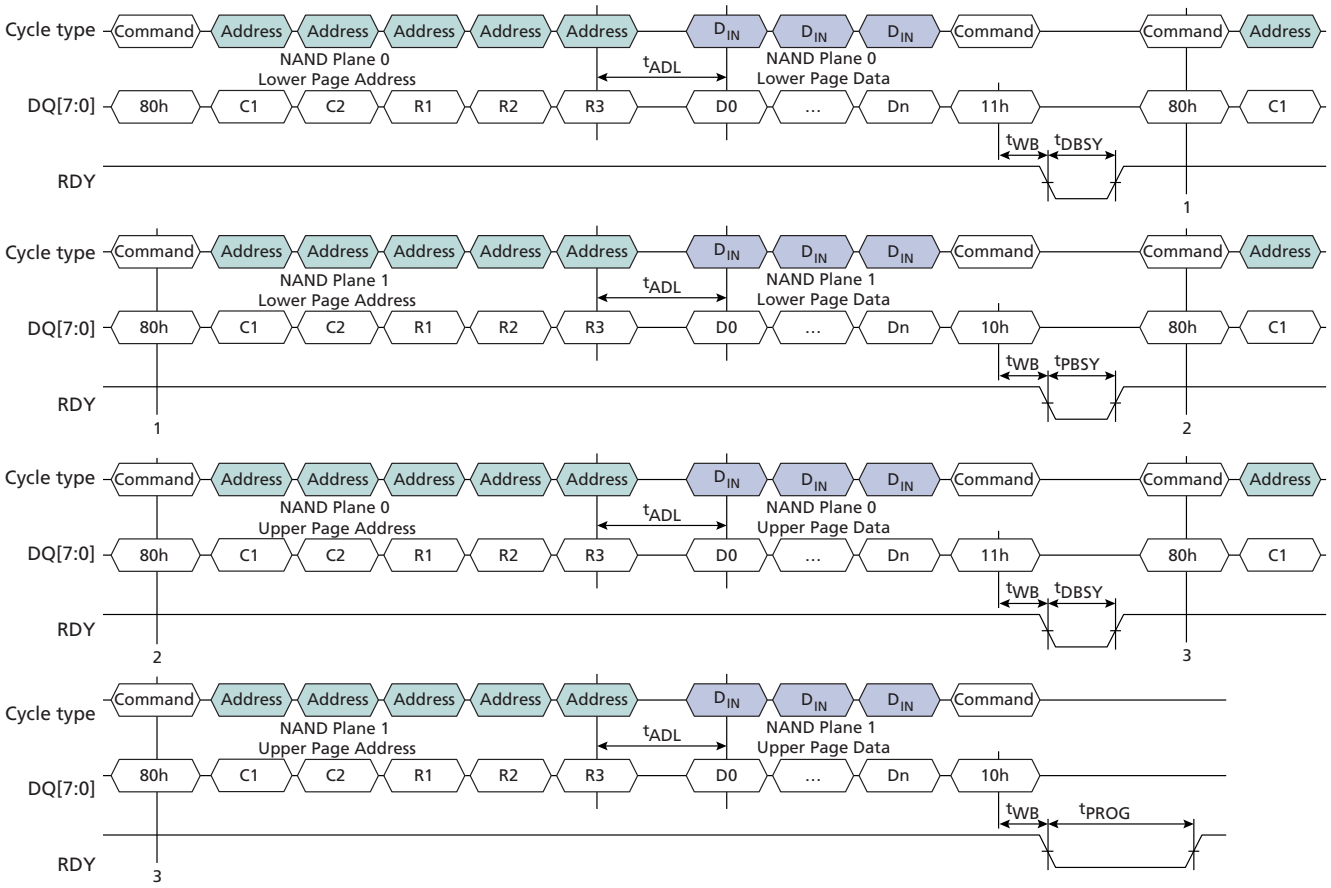
Additional PROGRAM PAGE MULTI-PLANE (80h-11h) commands can be issued to queue additional planes of lower page addresses for data transfer in this manner.

When the last address of lower page plane data is desired to be issued, instead of issuing the PROGRAM PAGE MULTI-PLANE (80h-11h) the PROGRAM PAGE (80h-10h) shall be issued. The selected LUN will go busy (RDY = 0, ARDY = 0) for ^{t}PBSY.

When the LUN's status shows that it is ready (RDY = 1) the same sequence that was use for inputting the lower page addresses for the previous inputted number of planes is repeated for the upper page addresses to complete the multi-plane programming sequence. When the final PROGRAM PAGE (80h-10h) command is issued with the last upper page address, data is transferred from the cache registers to the NAND Flash array for all of the addressed planes during ^{t}PROG. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the status of the FAIL bit for each of the planes to verify that programming completed successfully.

For the PROGRAM PAGE MULTI-PLANE (80h-11h) and PROGRAM PAGE (80h-10h) commands, see Multi-Plane Operations for multi-plane addressing requirements.

Figure 71: PROGRAM PAGE MULTI-PLANE (80h–11h) Operation



PROGRAM SUSPEND (84h) and PROGRAM RESUME (13h)

The PROGRAM SUSPEND (84h) command is used to pause a program in execution for the LUN specified (RDY = 0, ARDY = 0 or RDY = 1, ARDY = 0). If a PROGRAM SUSPEND (84h) command is issued when RDY (SR[6]) is set to one or zero and ARDY (SR[5]) is set to one or zero and the LUN is not performing a PROGRAM operation then the PROGRAM SUSPEND (84h) command should be ignored (for example, R/B# stays HIGH). If a multi-plane program is executing, the PROGRAM operation for all multi-plane addresses is paused and the LUN shall make forward progress for the PROGRAM operation prior to suspending the operation.

The SUSPEND (SR[2]) bit of the status register is valid for this command after ARDY transitions from zero to one and until the next array operation transition of RDY to zero or RESET (FFh, FCh, FAh, FDh) is issued. The FAIL (SR[0]) bit of the status register is valid for this command after ARDY transitions from zero to one until the next transition of ARDY to zero. SUSPEND shall be set to one if a program was suspended successfully, in this case FAIL (SR[0]) shall be cleared to zero. SR[2] shall be cleared to zero if the program was completed, in this case SR[0] reflects whether the program was successful.

Table 35: PROGRAM SUSPEND (84h) Status Details

Description	SR[2]	SR[1]	SR[0]
PROGRAM completed with successful status	0		
PROGRAM completed with fail status	0		
PROGRAM suspended	1		x (invalid)

To suspend an ongoing PROGRAM operation to a LUN, issue 84h command, then write five address cycles containing the row address (LUN, block and page address) and column addresses. Only the LUN address is required for program suspend; the block, page, and column addresses are ignored. The selected LUN status will be reflected in the status bits FAIL (SR[0]) and SUSPEND (SR[2]) in the status register after the status bit RDY is set to one. The selected LUN which the PROGRAM operation was suspended on will respond within ^{t}PSPD.

If issuing a program command while an ERASE operation on the same LUN is suspended, the PROGRAM operation is not allowed to be suspended.

To resume a suspended PROGRAM operation to a LUN, issue 13h command, then write five address cycles containing the row address matching the LUN in the suspended state; the block, page, and column addresses are ignored. The suspended PROGRAM operation will then resume and finish within ^{t}PROG.

While a program is suspended, if the host issues a RESET (FFh, FCh, FAh, FDh) command for the affected LUN, then the program that was suspended is canceled and status is cleared. With the exception of erase and program commands, all commands are allowed during suspended state (some with limitations listed in subsequent paragraphs). SET FEATURES (EFh) and SET FEATURES by LUN (D5h) commands are permitted during program suspend.

CACHE READ operations and read retry options that have a longer ^{t}R time are not permitted to be issued to a LUN that is in the program suspend state. Commands READ UNIQUE ID (EDh), READ OTP PAGE, and READ PARAMETER PAGE (ECh) are not allowed when the LUN is in a program suspend state.

While a program is suspended on a LUN, if host issues a PROGRAM (80h/81h-10h, 85h-10h) based command (regardless of the address) to the suspended LUN, the program command is not accepted by the LUN (R/B# goes LOW for ^{t}PSPDN) the LOCK status

(SR[7] = 0) is set and the program that was suspended keeps it's suspend state and can still be resumed. If a program based command is issued to a different LUN on the shared target then the program is performed on the selected page and the program that was suspended keeps its suspend state.

While a program is suspended, if host issues a read (00h-30h, 00h-31h, 00h-35h, 31h, 3Fh) based command to the page address (or any shared page) of the suspended program the read will be performed with data output being undefined and the program that was suspended keeps its suspend state. If host issues read command to block or LUN address other than the suspended page address then the read is performed and the program that was suspended keeps it's suspend state.

If the host issues a PROGRAM SUSPEND (84h) while there is no PROGRAM operation ongoing (including the case of the LUN already being in a program suspend state with SR[2]=1) the command should be ignored (for example, R/B# stays HIGH). If the host issues a PROGRAM RESUME (13h) while there is no PROGRAM operation ongoing or no program suspended, the NAND will respond with a ^{t}PSPDN busy time.

PROGRAM SUSPEND operations are only supported in the default mode of operation (for example, not in the OTP mode of operation).

Figure 72: PROGRAM SUSPEND (84h) Operation

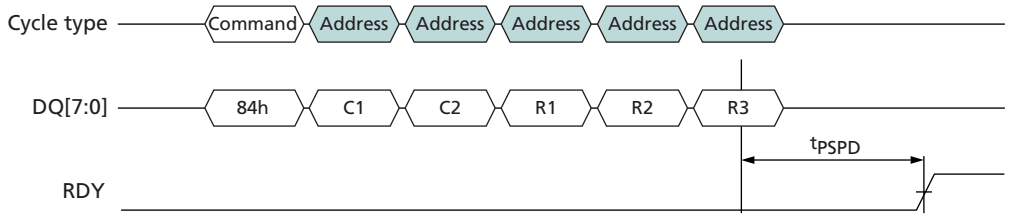
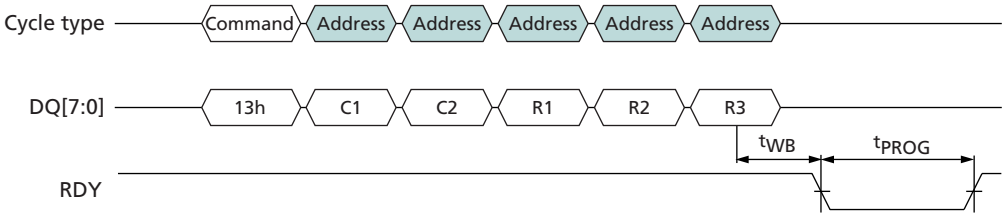


Figure 73: PROGRAM RESUME (13h) Operation



Erase Operations

Erase operations are used to clear the contents of a block in the NAND Flash array to prepare its pages for program operations.

ERASE Operations

The ERASE BLOCK (60h-D0h) command, when not preceded by the ERASE BLOCK MULTI-PLANE (60h-D1h) command, erases one block in the NAND Flash array. When the LUN is ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that this operation completed successfully.

MULTI-PLANE ERASE Operations

The ERASE BLOCK MULTI-PLANE (60h-D1h) command can be used to improve erase operation system performance by enabling multiple blocks to be erased in the NAND Flash array. This is done by prepending one or more ERASE BLOCK MULTI-PLANE (60h-D1h) commands in front of the ERASE BLOCK (60h-D0h) command. See Multi-Plane Operations for details.

ERASE BLOCK (60h–D0h)

The ERASE BLOCK (60h-D0h) command erases the specified block in the NAND Flash array. This command is accepted by the LUN when it is ready (RDY = 1, ARDY = 1).

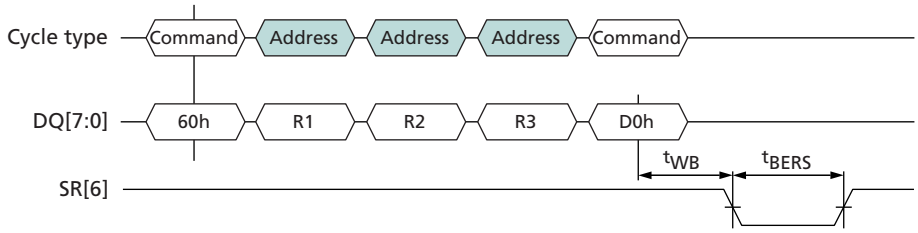
To erase a block, write 60h to the command register. Then write three address cycles containing the row address; the page address is ignored. Conclude by writing D0h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for ^{t}BERS while the block is erased.

To determine the progress of an ERASE operation, the host can monitor the target's R/B# signal, or alternatively, the status operations (70h, 78h) can be used. When the LUN is ready (RDY = 1, ARDY = 1) the host should check the status of the FAIL bit.

In devices that have more than one LUN per target, during and following multi-LUN operations, the READ STATUS ENHANCED (78h) command must be used to select only one LUN for status output. Use of the READ STATUS (70h) command could cause more than one LUN to respond, resulting in bus contention.

The ERASE BLOCK (60h-D0h) command is used as the final command of a MULTI-PLANE ERASE operation. It is preceded by one or more ERASE BLOCK MULTI-PLANE (60h-D1h) commands. All of blocks in the addressed planes are erased. The host should check the status of the operation by using the status operations (70h, 78h). See Multi-Plane Addressing for multi-plane addressing requirements.

Figure 74: ERASE BLOCK (60h–D0h) Operation



ERASE BLOCK MULTI-PLANE (60h–D1h)

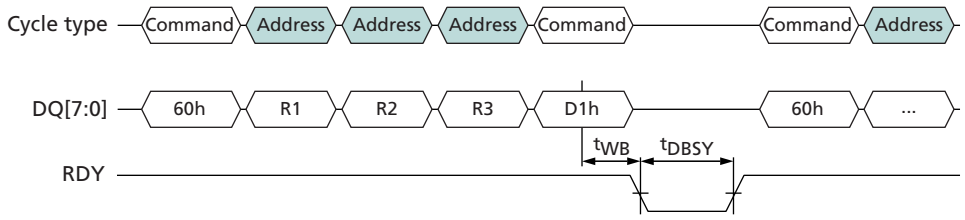
The ERASE BLOCK MULTI-PLANE (60h-D1h) command queues a block in the specified plane to be erased in the NAND Flash array. This command can be issued one or more times. Each time a new plane address is specified, that plane is also queued for a block to be erased. To specify the final block to be erased and to begin the erase operation for all previously queued planes, issue the ERASE BLOCK (60h-D0h) command. This command is accepted by the LUN when it is ready (RDY = 1, ARDY = 1).

To queue a block to be erased, write 60h to the command register, then write three address cycles containing the row address; the page address is ignored. Conclude by writing D1h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for ^{t}DBSY.

To determine the progress of ^{t}DBSY, the host can monitor the target's R/B# signal, or alternatively, the status operations (70h, 78h) can be used. When the LUN's status shows that it is ready (RDY = 1, ARDY = 1), additional ERASE BLOCK MULTI-PLANE (60h-D1h) commands can be issued to queue additional planes for erase. Alternatively, the ERASE BLOCK (60h-D0h) command can be issued to erase all of the queued blocks.

For the ERASE BLOCK MULTI-PLANE (60h-D1h) and ERASE BLOCK (60h-D0h) commands, see Multi-Plane Addressing for multi-plane addressing requirements.

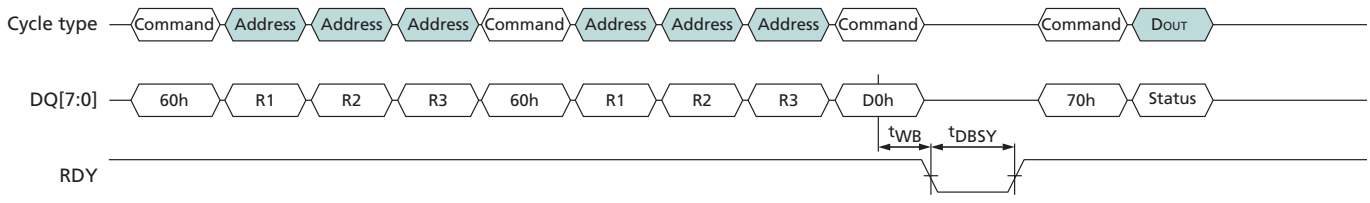
Figure 75: ERASE BLOCK MULTI-PLANE (60h–D1h) Operation



ERASE BLOCK MULTI-PLANE (60h–60h-D0h)

This operation behaves the same as the ERASE BLOCK MULTI-PLANE (60h-D1h) command followed by a ERASE BLOCK (60h-D0h) command.

Figure 76: ERASE BLOCK MULTI-PLANE (60h-60h-D0h) Operation



ERASE SUSPEND (61h) and ERASE RESUME (D2h)

The ERASE SUSPEND (61h) command is used to pause an erase in execution for the LUN specified (RDY =0, ARDY = 0). If ERASE SUSPEND (61h) is issued when ARDY = 1 or 0 and LUN is not performing an ERASE operation then the ERASE SUSPEND (61h) command should be ignored (for example, ^{t}ESPD = 0). If an interleaved erase is executing (ERASE operations on more than one LUN on a target), the erase for the addressed LUN with the ERASE SUSPEND (61h) command is paused. The LUN shall make forward progress for the erase prior to suspending (for example, complete an erase pulse). Since the erase is resumed from where it left off, an ERASE RESUME (D2h) on suspended block will count as one ERASE cycle. For example, if an erase is suspended and resumed twice it will count as three P/E cycles.

FAIL (SR[0]) and SUSPEND (SR[2]) of the status register are valid for this command after RDY transitions from zero to one until the next transition of RDY to zero. SR[2] shall be set to one if an erase was suspended successfully, in this case SR[0] shall be cleared to zero. SR[2] shall be cleared to zero if the erase was completed, in this case SR[0] reflects whether the erase was successful.

To suspend an ongoing ERASE operation to a LUN, write 61h to the command register, then write three address cycles containing the row address; the page address is ignored. The selected LUN status will be reflected in the status bits FAIL (SR[0]) and SUSPEND (SR[2]) in the status register after the status bit RDY (SR[6]) is set to one.

Table 36: ERASE SUSPEND (61h) Status Details

Description	SR[2]	SR[1]
ERASE completed with successful status	0	0
ERASE completed with fails status	0	1
ERASE suspended	1	0
Reserved	1	1

For multi-plane addressing requirements for the ERASE BLOCK MULTI-PLANE (60h-D1h) and ERASE BLOCK (60h-D0h) commands, see Multi-Plane Operations.

To resume a suspended ERASE operation issue the ERASE RESUME (D2h) command to the command register for the target (CE#) which has had an ERASE operation suspended. The suspended ERASE operation will then resume and finish within ^{t}BERS. In the case of Multi-LUN ERASE operations that have been suspended, the ERASE RESUME (D2h) command will cause all LUNs on a target (CE#) to resume any suspended ERASE operations.

While an erase is suspended, if the host issues a RESET (FFh, FCh, FAh) command for the affected LUN then the erase that was suspended is canceled and status is cleared. All commands are accepted during suspended state (some with limitations listed in subsequent paragraphs).

While an erase is suspended, if host issues a ERASE BLOCK (60h-D0h) command to the suspended block the suspended erase will be resumed (not restarted) and the erase that was suspended is canceled and status is cleared. If block erase is issued to different block address than suspended block then the erase is performed on the selected block and the erase that was suspended is canceled and status is cleared. If an erase is issued to a different LUN on the shared target then the erase is performed on the selected block and the erase that was suspended keeps it's suspend state.

Table 37: ERASE SUSPEND (61h) Behavior for ERASE Operations

Description	Command Issued	Next State
Block A ERASE operation suspended	ERASE BLOCK to block A	Resume ERASE operation to block A
	ERASE BLOCK to block B	Start normal erase to block B and suspend to block A is canceled
	ERASE BLOCK MULTI-PLANE to block A and B	Start normal erase to block A and B
ERASE BLOCK MULTI-PLANE to block A and B suspended	ERASE BLOCK to block A	Resume ERASE operation to block A and B
	ERASE BLOCK to block B	Resume ERASE operation to block A and B
	ERASE BLOCK MULTI-PLANE to block A and B	Resume ERASE operation to block A and B
	ERASE BLOCK MULTI-PLANE to block A and D	Start normal erase to block A and D. Suspend to block B is canceled
	ERASE BLOCK MULTI-PLANE to block C and B	Start normal erase to block C and B. Suspend to block A is canceled

While an erase is suspended, if host issues a program command to the suspended block or in the case of multi-plane program, if at least one of the blocks addressed has a suspended erase, the program is aborted with short busy time (^{t}ESPDN) and the LOCK status (SR[7] = 0) is set. In this case, the erase that was suspended keeps it's suspend state and can still be resumed. If host issues a program command to a block or LUN address other than the suspended block, also in case of a MULTI-PLANE PROGRAM operation, as long as the suspended block is not one of the addressed blocks, then the program is performed and the erase that was suspended keeps it's suspend state. The PROGRAM operation is not allowed to be suspended while there is a erase suspended for a given LUN that is in the erase suspend state.

While an erase is suspended, if host issues a read command to the suspended block the read will be performed (undefined data read out) and the erase that was suspended keeps it's suspend state. If host issues read command to block or LUN address other than the suspended block then the read is performed and the erase that was suspended keeps it's suspend state.

If the host issues an ERASE SUSPEND (61h) command while there is no ERASE operation ongoing the command should be ignored (for example, ^{t}ESPD = 0). If the host issues an ERASE RESUME (D2h) command while there is no ERASE operation ongoing or no erase suspended, the NAND will respond with a ^{t}ESPDN busy time. If the host issues an ERASE SUSPEND (61h) to a LUN already in erase suspend state, the command will be ignored and the erase that was suspended will stay in the erase suspend state.

It is recommended for forward progress to occur on an ERASE SUSPEND (61h) operation, the host should not issue two consecutive ERASE SUPSEND (61h) commands within 1ms of each other. If repeated ERASE SUSPEND (61h) commands are issued less than 1ms apart the ERASE operation may not complete.

Figure 77: ERASE SUSPEND (61h) Operation

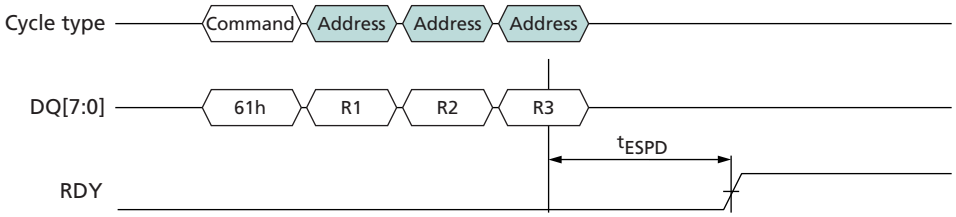
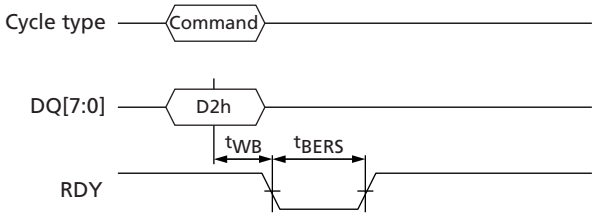


Figure 78: ERASE RESUME (D2h) Operation



COPYBACK Operations

COPYBACK operations make it possible to transfer data within a plane from one page to another using the cache register. This is particularly useful for block management and wear leveling.

The COPYBACK operation is a two-step process consisting of a COPYBACK READ (00h-35h) and a COPYBACK PROGRAM (85h-10h) command. To move data from one page to another on the same plane, first issue the COPYBACK READ (00h-35h) command. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host can transfer the data to a new page by issuing the COPYBACK PROGRAM (85h-10h) command. When the die (LUN) is again ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that this operation completed successfully.

To prevent bit errors from accumulating over multiple COPYBACK operations, it is recommended that the host read the data out of the cache register after the COPYBACK READ (00h-35h) completes prior to issuing the COPYBACK PROGRAM (85h-10h) command. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address. The host should check the data for ECC errors and correct them. When the COPYBACK PROGRAM (85h-10h) command is issued, any corrected data can be input. The CHANGE ROW ADDRESS (85h) command can be used to change the column address.

It is not possible to use the COPYBACK operation to move data from one plane to another or from one die (LUN) to another. Instead, use a READ PAGE (00h-30h) or COPYBACK READ (00h-35h) command to read the data out of the NAND, and then use a PROGRAM PAGE (80h-10h) command with data input to program the data to a new plane or die (LUN).

Between the COPYBACK READ (00h-35h) and COPYBACK PROGRAM (85h-10h) commands, the following commands are supported: STATUS operations (70h, 78h), and column address operations (05h-E0h, 06h-E0h, 85h). RESET operations (FFh, FCh) can be issued after COPYBACK READ (00h-35h), but the contents of the cache registers on the target are not valid.

In devices which have more than one die (LUN) per target, once the COPYBACK READ (00h-35h) is issued, interleaved die (multi-LUN) operations are prohibited until after the COPYBACK PROGRAM (85h-10h) command is issued.

MULTI-PLANE COPYBACK Operations

MULTI-PLANE COPYBACK READ operations improve read data throughput by copying data simultaneously from more than one plane to the specified cache registers. This is done by prepending one or more READ PAGE MULTI-PLANE (00h-32h) commands in front of the COPYBACK READ (00h-35h) command.

The COPYBACK PROGRAM MULTI-PLANE (85h-11h) command can be used to further system performance of COPYBACK PROGRAM operations by enabling movement of multiple pages from the cache registers to different planes of the NAND Flash array. This is done by prepending one or more COPYBACK PROGRAM (85h-11h) commands in front of the COPYBACK PROGRAM (85h-10h) command. See Multi-Plane Operations for details.

COPYBACK READ (00h–35h)

The COPYBACK READ (00h-35h) command is functionally identical to the READ PAGE (00h-30h) command, except that 35h is written to the command register instead of 30h. See READ PAGE (00h-30h) for further details.

Though it is not required, it is recommended that the host read the data out of the device to verify the data prior to issuing the COPYBACK PROGRAM (85h-10h) command to prevent the propagation of data errors.

Figure 79: COPYBACK READ (00h–35h) Operation

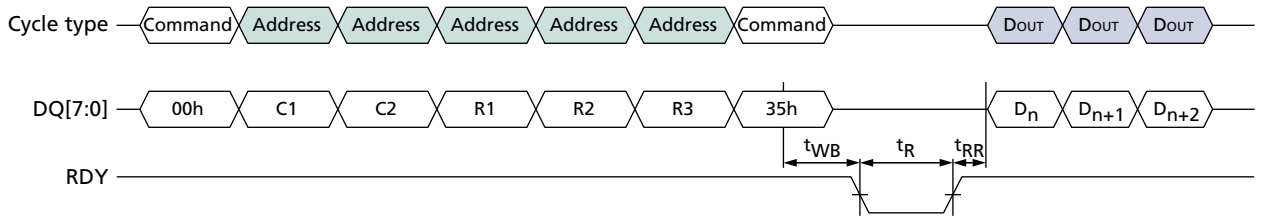
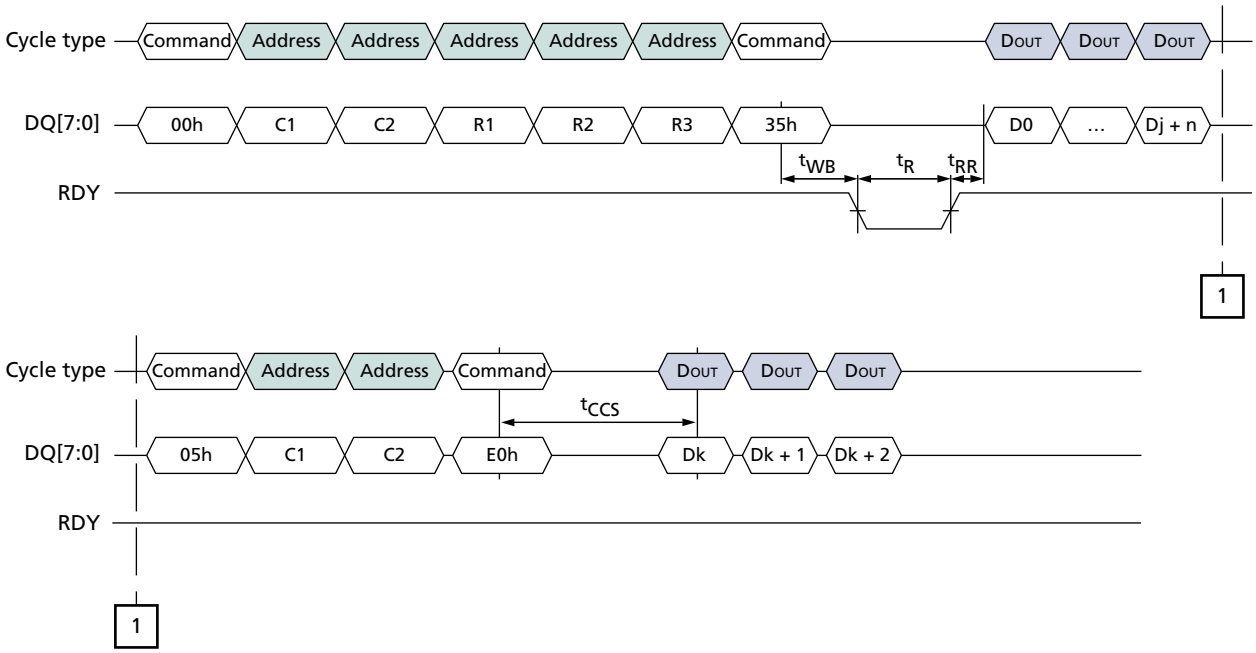


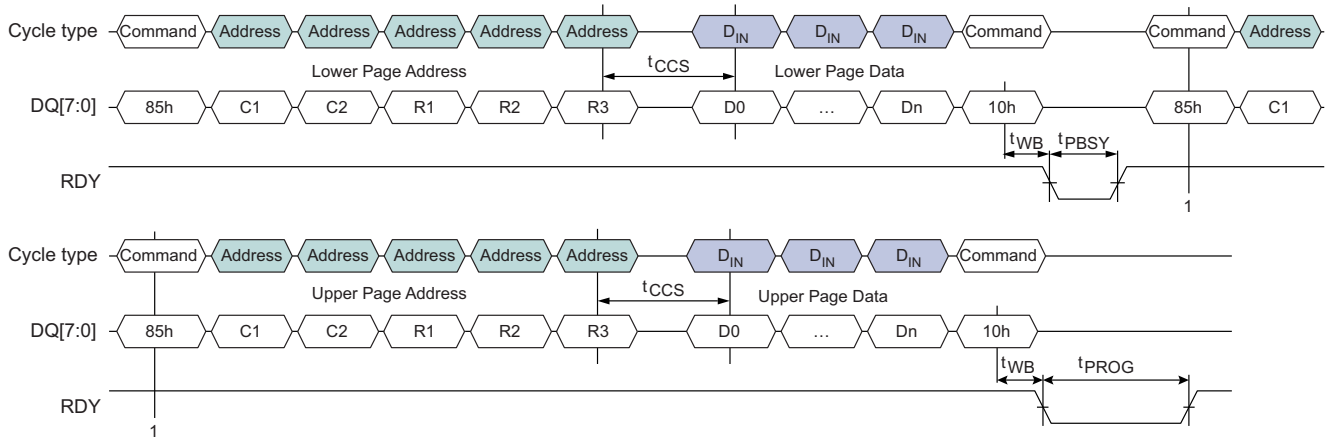
Figure 80: COPYBACK READ (00h–35h) with CHANGE READ COLUMN (05h–E0h) Operation



COPYBACK PROGRAM (85h–10h)

The COPYBACK PROGRAM (85h-10h) command is functionally identical to the PROGRAM PAGE (80h-10h) command, except that when 85h is written to the command register, cache register contents are not cleared. See PROGRAM PAGE (80h-10h) for further details.

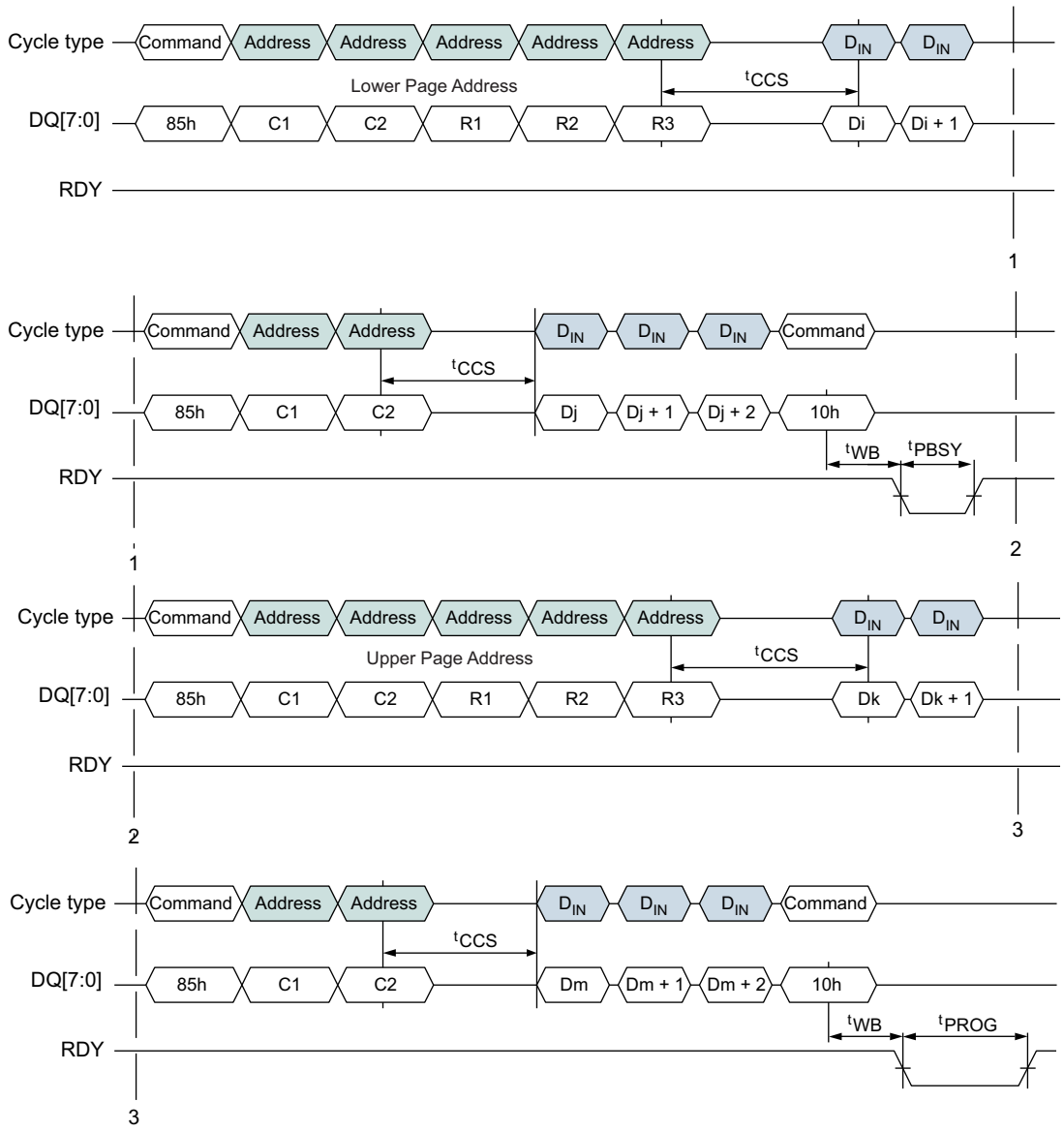
Figure 81: COPYBACK PROGRAM (85h–10h) Operation – Single-Pass



Example command sequence for COPYBACK PROGRAM with Single Pass Programming Enabled:

1. Issue COPYBACK READ (00h-35h) (It is possible for the COPYBACK READ (00h-35h) command to address a different block or page type from the subsequent 85h command, however both the 00h-35h and 85h commands must address the same plane.)
2. Read data out and identify errors (optional)
3. Issue CHANGE WRITE COLUMN (85h) + 5 address cycles (addressed to a lower page) to address of first error and enter corrected data. Repeat error correction by issuing CHANGE WRITE COLUMN (85h) + 2 column address cycles until all errors are corrected, then issue 10h command.
4. Wait ^{t}PBSY
5. Issue COPYBACK READ (00h-35h) to another address
6. Read data out and identify errors (optional)
7. Issue CHANGE WRITE COLUMN (85h) + 5 address cycles (addressed to an upper page) to address of first error and enter corrected data. Repeat error correction by issuing CHANGE WRITE COLUMN (85h) + 2 column address cycles until all errors are corrected, then issue 10h command.
8. Wait ^{t}PROG

Figure 82: COPYBACK PROGRAM (85h-10h) with CHANGE WRITE COLUMN (85h) Operation – Single-Pass



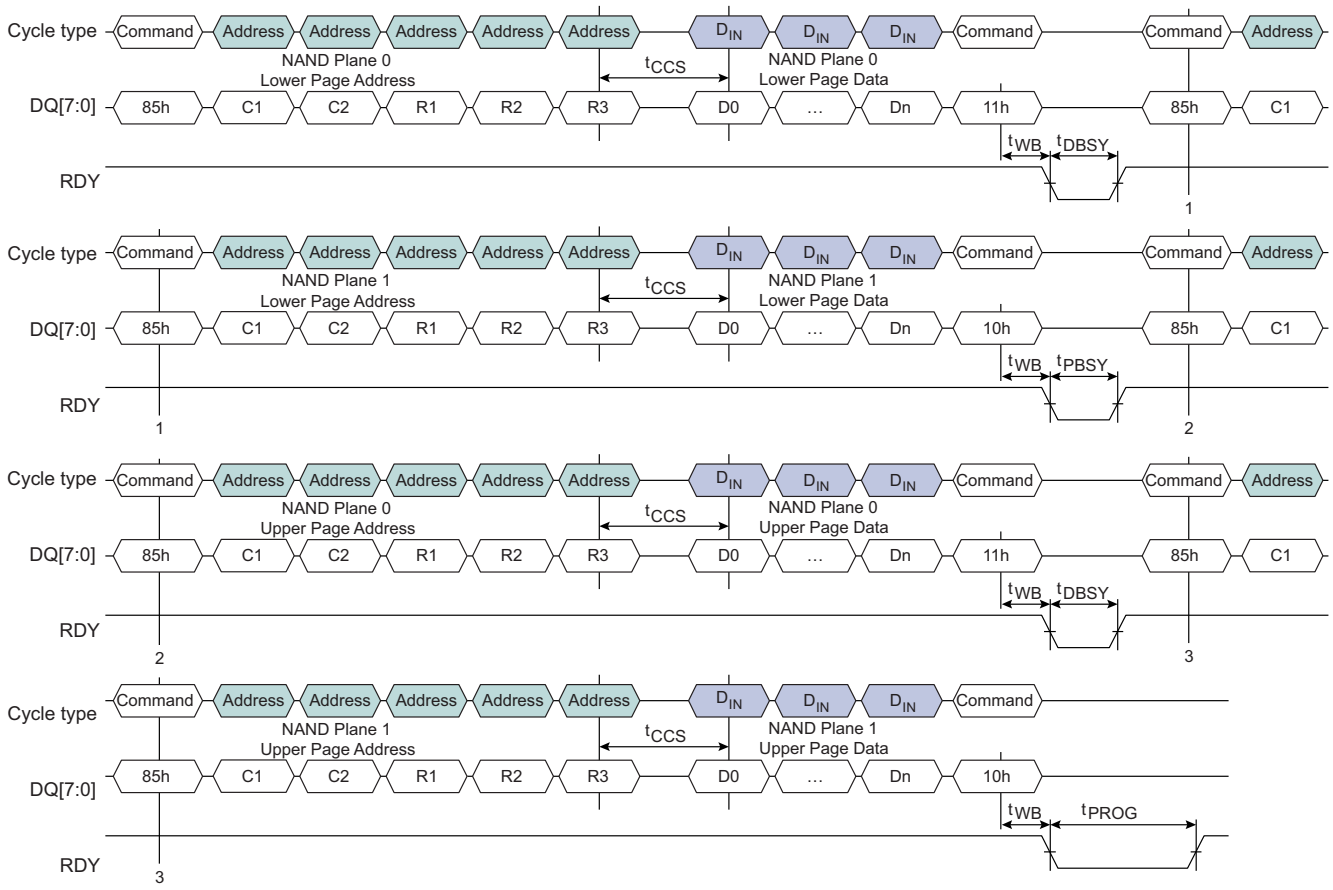
COPYBACK READ MULTI-PLANE (00h-32h)

The COPYBACK READ MULTI-PLANE (00h-32h) command is functionally identical to the READ PAGE MULTI-PLANE (00h-32h) command, except that the 35h command is written as the final command. The complete command sequence for the COPYBACK READ PAGE MULTI-PLANE is 00h-32h-00h-35h. See Read Operation - READ PAGE MULTI-PLANE (00h-32h) section for further details.

COPYBACK PROGRAM MULTI-PLANE (85h-11h)

The COPYBACK PROGRAM MULTI-PLANE (85h-11h) command is functionally identical to the PROGRAM PAGE MULTI-PLANE (80h-11h) command, except that when 85h is written to the command register, cache register contents are not cleared. See PROGRAM PAGE MULTI-PLANE (80h-11h) for further detail.

Figure 83: COPYBACK PROGRAM MULTI-PLANE (85h-11h) Operation – Single-Pass



Multi-Plane Operations

Each NAND Flash logical unit (LUN) is divided into multiple physical planes. Each plane contains a cache register and a data register independent of the other planes. The planes are addressed via the low-order block address bits. Specific details are provided in Device and Array Organization.

Multi-plane operations make better use of the NAND Flash arrays on these physical planes by performing concurrent READ, PROGRAM, or ERASE operations on multiple planes, significantly improving system performance. Multi-plane operations must be of the same type across the planes; for example, it is not possible to perform a PROGRAM operation on one plane with an ERASE operation on another.

When issuing MULTI-PLANE PROGRAM operation, use the READ STATUS (70h) command and check whether the previous operation(s) failed. If the READ STATUS (70h) command indicates that an error occurred (FAIL=1 and/or FAILC =1), use the READ STATUS ENHANCED (78h) command—time for each plane—to determine which plane operation failed.

When issuing MULTI-PLANE ERASE operations, use the READ STATUS (70h) command and check whether the previous operation(s) failed. If the READ STATUS (70h) command indicates that an error occurred (FAIL=1), use the READ STATUS ENHANCED (78h) command—time for each plane—to determine which plane operation failed.

Multi-Plane Addressing

Multi-plane commands require multiple addresses, one address per operational plane. For a given multi-plane operation, these addresses are subject to the following requirements:

- The LUN address bit(s) must be identical for all of the issued addresses.
- The plane select bit, BA[8], must be different for each issued address.
- The page address bits, PA[7:0], must be identical for all the issued addresses.

The READ STATUS (70h) command should be used following MULTI-PLANE PROGRAM PAGE and ERASE BLOCK operations on a single LUN.

Interleaved Die (Multi-LUN) Operations

In devices that have more than one die (LUN) per target, it is possible to improve performance by interleaving operations between the die (LUNs). An interleaved die (multi-LUN) operation is one that individual die (LUNs) involved may be in any combination of busy or ready status during operations.

Interleaved die (multi-LUN) operations are prohibited following RESET (FFh, FCh), identification (90h, ECh, EDh), and configuration (EEh, EFh) operations until ARDY = 1 for all of the die (LUNs) on the target.

During an interleaved die (multi-LUN) operation, there are two methods to determine operation completion. The R/B# signal indicates when all of the die (LUNs) have finished their operations. R/B# remains LOW while any die (LUN) is busy. When R/B# goes HIGH, all of the die (LUNs) are idle and the operations are complete. Alternatively, the READ STATUS ENHANCED (78h) command can report the status of each die (LUN) individually.

If a die (LUN) is performing a cache operation, like PROGRAM PAGE CACHE (80h-15h), then the die (LUN) is able to accept the data for another cache operation when status register bit 6 is 1. All operations, including cache operations, are complete on a die when status register bit 5 is 1.

Use the READ STATUS ENHANCED (78h) command to monitor status for the addressed die (LUN). When multi-plane commands are used with interleaved die (multi-LUN) operations, the multi-plane commands must also meet the requirements, see Multi-Plane Operations for details. After the READ STATUS ENHANCED (78h) command has been issued, the READ STATUS (70h) command may be issued for the previously addressed die (LUN).

See Command Definitions for the list of commands that can be issued while other die (LUNs) are busy.

During an interleaved die (multi-LUN) operation that involves a PROGRAM-series (80h-10h, 80h-15h, 80h-11h) operation and a READ operation, the PROGRAM-series operation must be issued before the READ-series operation. The data from the READ-series operation must be output to the host before the next PROGRAM-series operation is issued. This is because the 80h command clears the cache register contents of all cache registers on all planes.

During a interleaved die (multi-LUN) operation that involves PROGRAM-series (80h-10h, 80h-15h, 80h-11h) operations between multiple die (LUNs) on the same target, after data is inputted to the first die (LUN) addressed in that interleaved die (multi-LUN) sequence, before addressing the next die (LUN) with a PROGRAM-series (80h-10h, 80h-15h, 80h-11h) operation a program confirm command (via 80h-10h, 80-15h) must be issued to begin the array programming of the die (LUN). If this is not done by the host prior to addressing the next die (LUN), data in all the cache registers of the previously die (LUNs) will be cleared by the PROGRAM-series (80h-10h, 80h-15h, 80h-11h) operation to the next die (LUN) in the interleaved die (multi-LUN) sequence. Utilizing the Program Clear functionality in feature address 01h can be utilized to avoid a PROGRAM-series (80h-10h, 80h-15h, 80h-11h) operation from clearing the contents of non-addressed NAND planes.

When issuing combinations of commands to multiple die (LUNs) (for example, Reads to one die (LUN) and Programs to another die (LUN)) or Reads to one die (LUN) and Reads to another die (LUN)), the host shall issue the READ STATUS ENHANCED (78h) command before reading data from any LUN. This ensures that only the LUN selected by the READ STATUS ENHANCED (78h) command responds to a data output cycle after being put into data output mode, and thus avoiding bus contention. After the READ STATUS

ENHANCED (78h) command is issued to the selected die (LUN) a CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h) command shall be issued prior to any data output from the selected die (LUN).

Error Management

Each NAND Flash die (LUN) is specified to have a minimum number of valid blocks (NVB) of the total available blocks. This means the die (LUNs) could have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional blocks can develop with use. However, the total number of available blocks per die (LUN) will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices could contain bad blocks, they can be used quite reliably in systems that provide bad-block management and error-correction algorithms. This type of software environment ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI Factory Defect Mapping requirements. See the following table for the first spare area location and the bad-block mark.

System software should check the first spare area location on the first page of each block prior to performing any PROGRAM or ERASE operations on the NAND Flash device. A bad block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks could be marginal, it may not be possible to recover this information if the block is erased.

Over time, some memory locations may fail to program or erase properly. In order to ensure that data is stored properly over the life of the NAND Flash device, the following precautions are required:

- Always check status after a PROGRAM or ERASE operation
- Under typical conditions, use the minimum required ECC (see table below)
- Use bad-block management and wear-leveling algorithms

The first block (physical block address 00h) for each CE# is guaranteed to be valid with ECC when shipped from the factory.

Table 38: Error Management Details

Description	Requirement
Minimum number of valid blocks (NVB) per LUN	See Table 59, Valid Blocks per LUN
Total available blocks per LUN	2192
First spare area location	Byte 16,384
Bad-block mark	00h
Minimum required ECC	72-bit ECC per 1162 bytes of data

Shared Pages

In MLC NAND Flash devices, each memory cell contains two bits of data. These bits are distributed across two NAND pages. Pages within a NAND block that share the same NAND memory cells are referred to as shared pages. If any PROGRAM operation is interrupted (for example, power loss or reset), data in previously programmed shared pages can also be corrupted.

The least significant numbered shared page must be programmed before the most significant numbered page of that pair can be programmed.

Table 39: Shared Pages

Shared Pages		Shared Pages		Shared Pages		Shared Pages	
0	–	1	–	2	–	3	–
4	–	5	–	6	–	7	–
8	–	9	–	10	–	11	–
12	–	13	–	14	–	15	–
16	17	18	19	20	21	22	23
24	25	26	27	28	29	30	31
32	33	34	35	36	37	38	39
40	41	42	43	44	45	46	47
48	49	50	51	52	53	54	55
56	57	58	59	60	61	62	63
64	65	66	67	68	69	70	71
72	73	74	75	76	77	78	79
80	81	82	83	84	85	86	87
88	89	90	91	92	93	94	95
96	97	98	99	100	101	102	103
104	105	106	107	108	109	110	111
112	113	114	115	116	117	118	119
120	121	122	123	124	125	126	127
128	129	130	131	132	133	134	135
136	137	138	139	140	141	142	143
144	145	146	147	148	149	150	151
152	153	154	155	156	157	158	159
160	161	162	163	164	165	166	167
168	169	170	171	172	173	174	175
176	177	178	179	180	181	182	183
184	185	186	187	188	189	190	191
192	193	194	195	196	197	198	199
200	201	202	203	204	205	206	207
208	209	210	211	212	213	214	215
216	217	218	219	220	221	222	223
224	225	226	227	228	229	230	231
232	233	234	235	236	237	238	239
240	241	242	243	244	245	246	247
248	249	250	251	252	253	254	255
256	257	258	259	260	261	262	263
264	265	266	267	268	269	270	271
272	273	274	275	276	277	278	279

Table 39: Shared Pages

Shared Pages		Shared Pages		Shared Pages		Shared Pages	
280	281	282	283	284	285	286	287
288	289	290	291	292	293	294	295
296	297	298	299	300	301	302	303
304	305	306	307	308	309	310	311
312	313	314	315	316	317	318	319
320	321	322	323	324	325	326	327
328	329	330	331	332	333	334	335
336	337	338	339	340	341	342	343
344	345	346	347	348	349	350	351
352	353	354	355	356	357	358	359
360	361	362	363	364	365	366	367
368	369	370	371	372	373	374	375
376	377	378	379	380	381	382	383
384	385	386	387	388	389	390	391
392	393	394	395	396	397	398	399
400	401	402	403	404	405	406	407
408	409	410	411	412	413	414	415
416	417	418	419	420	421	422	423
424	425	426	427	428	429	430	431
432	433	434	435	436	437	438	439
440	441	442	443	444	445	446	447
448	449	450	451	452	453	454	455
456	457	458	459	460	461	462	463
464	465	466	467	468	469	470	471
472	473	474	475	476	477	478	479
480	481	482	483	484	485	486	487
488	489	490	491	492	493	494	495
496		497		498		499	
500		501		502		503	
504		505		506		507	
508		509		510		511	

Output Drive Impedance

Because NAND Flash is designed for use in systems that are typically point-to-point connections, an option to control the drive strength of the output buffers is provided. Drive strength should be selected based on the expected loading of the memory bus. The three supported settings for the output drivers for the asynchronous, NV-DDR, and NV-DDR2 interfaces are: 25 ohms, 35 ohms, and 50 ohms.

The 35 ohm output drive strength setting is the power-on default value in the asynchronous, NV-DDR, and NV-DDR2 interfaces. The host can select a different drive strength setting using the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command.

The output impedance range from minimum-to-maximum covers process, voltage, and temperature variations. Devices are not guaranteed to be at the nominal line.

Table 40: Output Drive Strength Test Conditions (V_{CCQ} = 1.7–1.95V)

Range	Process	Voltage	Temperature
Minimum	Fast-Fast	1.95V	T_{OPER} (MIN)
Nominal	Typical-Typical	1.8V	+25°C
Maximum	Slow-Slow	1.7V	T_{OPER} (MAX)

Table 41: Output Drive Strength Impedance Values (V_{CCQ} = 1.7–1.95V)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
25 Ohms	Rpd	V_{CCQ} × 0.2	11.4	25.0	44.0	Ohms
		V_{CCQ} × 0.5	15.0	25.0	44.0	Ohms
		V_{CCQ} × 0.8	15.0	25.0	61.0	Ohms
	Rpu	V_{CCQ} × 0.2	15.0	25.0	61.0	Ohms
		V_{CCQ} × 0.5	15.0	25.0	44.0	Ohms
		V_{CCQ} × 0.8	11.4	25.0	44.0	Ohms
35 Ohms	Rpd	V_{CCQ} × 0.2	16.0	35.0	61.0	Ohms
		V_{CCQ} × 0.5	21.0	35.0	61.0	Ohms
		V_{CCQ} × 0.8	21.0	35.0	85.3	Ohms
	Rpu	V_{CCQ} × 0.2	21.0	35.0	85.3	Ohms
		V_{CCQ} × 0.5	21.0	35.0	61.0	Ohms
		V_{CCQ} × 0.8	16.0	35.0	61.0	Ohms
50 Ohms	Rpd	V_{CCQ} × 0.2	24.0	50.0	87.0	Ohms
		V_{CCQ} × 0.5	30.0	50.0	87.0	Ohms
		V_{CCQ} × 0.8	30.0	50.0	122.0	Ohms
	Rpu	V_{CCQ} × 0.2	30.0	50.0	122.0	Ohms
		V_{CCQ} × 0.5	30.0	50.0	87.0	Ohms
		V_{CCQ} × 0.8	24.0	50.0	87.0	Ohms

Table 42: Pull-Up and Pull-Down Output Impedance Mismatch for Asynchronous, NV-DDR, and NV-DDR2

Drive Strength	Minimum	Maximum	Notes
25 Ohms	0	4.4	1, 2
35 Ohms	0	6.2	1, 2
50 Ohms	0	8.8	1, 2

Notes: 1. Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.
2. Test conditions: $V_{CCQ} = V_{CCQ}(MIN)$, $V_{OUT} = V_{CCQ} \times 0.5$, $T_A = T_{OPER}$.

AC Overshoot/Undershoot Specifications

The supported AC overshoot and undershoot area depends on the timing mode selected by the host. NAND devices may have different maximum amplitude requirements for overshoot and undershoot than the host controller. If the host controller has more stringent requirements, termination, or other means of reducing overshoot or undershoot may be required beyond the NAND requirements.

Table 43: Asynchronous Overshoot / Undershoot Parameters

Parameter	Timing Mode						Unit
	0	1	2	3	4	5	
Maximum peak amplitude provided for overshoot area	1	1	1	1	1	1	V
Maximum peak amplitude provided for undershoot area	1	1	1	1	1	1	V
Maximum overshoot are above V_{CCQ}	3	3	3	3	3	3	V-ns
Maximum undershoot area below V_{SSQ}	3	3	3	3	3	3	V-ns

Table 44: NV-DDR Overshoot / Undershoot Parameters

Parameter	Timing Mode						Unit
	0	1	2	3	4	5	
Maximum peak amplitude provided for overshoot area	1	1	1	1	1	1	V
Maximum peak amplitude provided for undershoot area	1	1	1	1	1	1	V
Maximum overshoot are above V_{CCQ}	3	3	3	2.25	1.8	1.5	V-ns
Maximum undershoot area below V_{SSQ}	3	3	3	2.25	1.8	1.5	V-ns

Table 45: NV-DDR2 Overshoot / Undershoot Parameters

Parameter	Signals	Timing Mode									Unit
		0	1	2	3	4	5	6	7	8	
Maximum peak amplitude provided for overshoot area	–	1	1	1	1	1	1	1	1	1	V
Maximum peak amplitude provided for undershoot area	–	1	1	1	1	1	1	1	1	1	V
Maximum overshoot are above V_{CCQ}	DQ[7:0], DQS, RE#	3	3	2.25	1.8	1.5	1.1	0.9	0.75	0.56	V-ns
	ALE, CLE, WE#	3	3	3	3	3	3	3	3	3	
Maximum undershoot area below V_{SSQ}	DQ[7:0], DQS, RE#	3	3	2.25	1.8	1.5	1.1	0.9	0.75	0.56	V-ns
	ALE, CLE, WE#	3	3	3	3	3	3	3	3	3	

Figure 84: Overshoot

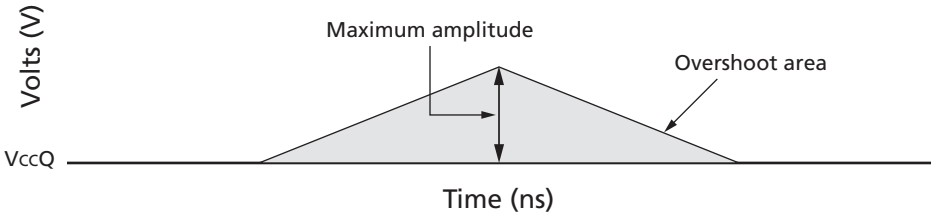
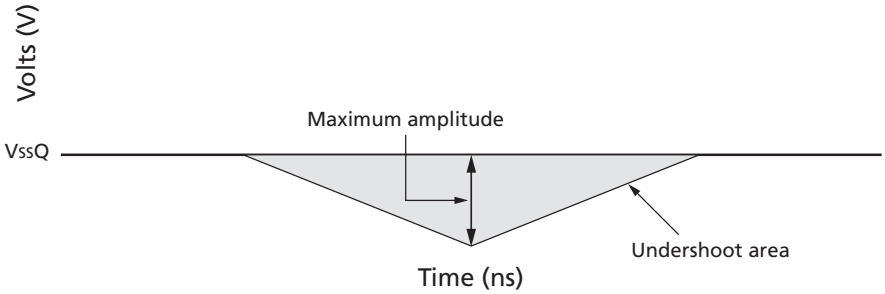


Figure 85: Undershoot



Input Slew Rate

Though all AC timing parameters are tested with a nominal input slew rate of 1V/ns, it is possible to run the device at a slower slew rate. The input slew rates shown below are sampled, and not 100% tested. If using slew rates slower than the minimum values, timing must be derated by the host.

Table 46: Test Conditions for Input Slew Rate

Parameter	Value
Rising edge for setups	$V_{IL(DC)}$ to $V_{IH(AC)}$ for NV-DDR
	The last crossing of $V_{REFQ(DC)}$ and the first crossing of $V_{IH(AC)}$ min for NV-DDR2
Falling edge for setups	$V_{IH(DC)}$ to $V_{IL(AC)}$ for NV-DDR
	The last crossing of $V_{REFQ(DC)}$ and the first crossing of $V_{IL(AC)}$ max for NV-DDR2
Rising edge for holds	$V_{IL(DC)}$ to $V_{IH(AC)}$ for NV-DDR
	The first crossing of $V_{IL(DC)}$ max and the first crossing of $V_{REFQ(DC)}$ for NV-DDR2
Falling edge for holds	$V_{IH(DC)}$ to $V_{IL(AC)}$ for NV-DDR
	The first crossing of $V_{IH(DC)}$ min and the first crossing of $V_{REFQ(DC)}$ for NV-DDR2
Temperature Range	T_{OPER}

The minimum and maximum input slew rate requirements that the device shall comply with below for NV-DDR operations. If the input slew rate falls below the minimum value, then derating shall be applied.

Table 47: NV-DDR Maximum and Minimum Input Slew Rate

Description	Timing Modes 0-5	Unit
Input slew rate (min)	0.5	V/ns
Input slew rate (max)	4.5	V/ns

Table 48: Input Slew Rate derating for NV-DDR (V_{CCQ} = 1.7–1.95V)

Command/ Address and DQ V/ns	Δ^tDS, Δ^tDH Derating $V_{IH(AC)}/V_{IL(AC)}$= V_{REF} ±540mV, $V_{IH(DC)}/V_{IL(DC)}$ = V_{REF} ±360mV																Unit
	CLK/DQS Slew Rate																
	1 V/ns		0.9 V/ns		0.8 V/ns		0.7 V/ns		0.6 V/ns		0.5 V/ns		0.4 V/ns		0.3 V/ns		
	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	
1	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	ps
0.9	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	
0.8	-	-	0	0	0	0	0	0	-	-	-	-	-	-	-	-	
0.7	-	-	-	-	0	0	0	0	0	0	-	-	-	-	-	-	
0.6	-	-	-	-	-	-	0	0	0	0	0	0	-	-	-	-	
0.5	-	-	-	-	-	-	-	-	0	0	0	0	180	180	-	-	
0.4	-	-	-	-	-	-	-	-	-	-	180	180	360	360	660	660	
0.3	-	-	-	-	-	-	-	-	-	-	-	-	660	660	920	920	

The minimum and maximum input slew rate requirements that the device shall comply with below for NV-DDR2 operations. If the input slew rate falls below the minimum value, then derating shall be applied.

Table 49: NV-DDR2 Maximum and Minimum Input Slew Rate

	Single Ended	Differential	
Description	**Timing Modes 0-7**	**Timing Modes 0-7**	**Unit**
Input slew rate (min)	1.0	2.0	V/ns
Input slew rate (max)	4.5	9.0	V/ns

For DQ signals when used for input, the total data setup time (^{t}DS) and data hold time (^{t}DH) required is calculated by adding a derating value to the ^{t}DS and ^{t}DH values indicated for the timing mode. To calculate the total data setup time, ^{t}DS is incremented by the appropriate Δset derating value. To calculate the total data hold time, ^{t}DH is incremented by the appropriate Δhold derating value. Table 50 and Input Slew Rate provides the derating values when single-ended DQS is used. Table 51 and Input Slew Rate provides the derating values when differential DQS (DQS_t/DQS_c) is used.

The setup nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REFQ(DC)}$ and the first crossing of $V_{IH(AC)}$ min. The setup nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REFQ(DC)}$ and the first crossing of $V_{IL(AC)}$ max. If the actual signal is always earlier than the nominal slew rate line between the shaded '$V_{REFQ(DC)}$ to AC region', then the derating value uses the nominal slew rate shown in Figure 86. If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REFQ(DC)}$ to AC region', then the derating value uses the slew rate of a tangent line to the actual signal from the AC level to the DC level shown in Figure 87.

The hold nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)}$ max and the first crossing of $V_{REFQ(DC)}$. The hold nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)}$ min and the first crossing of $V_{REFQ(DC)}$. If the actual signal is always later than the nominal slew rate line between shaded 'DC to $V_{REFQ(DC)}$ region', then the derating value uses the nominal slew rate shown in Figure 88. If the actual signal is earlier than the nominal slew rate line anywhere between the shaded 'DC to $V_{REFQ(DC)}$ region', then the derating value uses the slew rate of a tangent line to the actual signal from the DC level to the $V_{REFQ(DC)}$ level shown in Figure 89.

If the tangent line is used for derating, the setup and hold values shall be derated from where the tangent line crosses $V_{REFQ(DC)}$, not the actual signal (refer to Figure 87 and Figure 89).

For slew rates not explicitly listed in Figure 50 and Figure 51, the derating values should be obtained by linear interpolation. These values are typically not subject to production test; the values are verified by design and characterization.

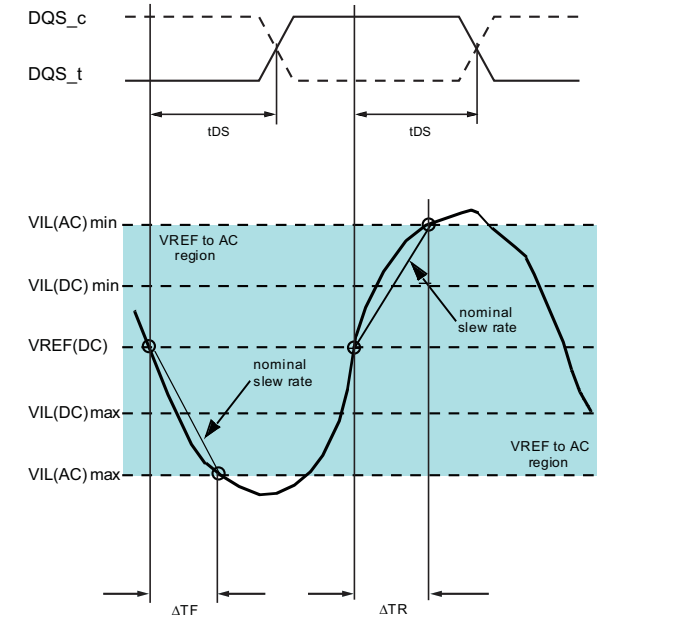
Table 50: Input Slew Rate derating for NV-DDR2 single-sided (V_{CCQ} = 1.7–1.95V)

DQ V/ns	Δ^tDS, Δ^tDH Derating (ps) $V_{IH(AC)}/V_{IL(AC)}$= V_{REF} ±250mV, $V_{IH(DC)}/V_{IL(DC)}$ = V_{REF} ±125mV																				Unit
	ΔDQS Slew Rate																				
	2 V/ns		1.5 V/ns		1 V/ns		0.9 V/ns		0.8 V/ns		0.7 V/ns		0.6 V/ns		0.5 V/ns		0.4 V/ns		0.3 V/ns		
	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	
2	0	0	0	0	0	0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ps
1.5	0	0	0	0	0	0	14	0	–	–	–	–	–	–	–	–	–	–	–	–	ps
1	0	0	0	0	0	0	14	0	31	0	–	–	–	–	–	–	–	–	–	–	ps
0.9	–	–	14	0	14	0	28	0	45	0	67	0	–	–	–	–	–	–	–	–	ps
0.8	–	–	–	–	31	0	45	0	63	0	85	0	115	0	–	–	–	–	–	–	ps
0.7	–	–	–	–	–	–	67	0	85	0	107	0	137	0	179	0	–	–	–	–	ps
0.6	–	–	–	–	–	–	–	–	115	0	137	0	167	0	208	0	271	0	–	–	ps
0.5	–	–	–	–	–	–	–	–	–	–	179	0	208	0	250	0	313	0	418	0	ps
0.4	–	–	–	–	–	–	–	–	–	–	–	–	271	0	313	0	375	0	480	0	ps
0.3	–	–	–	–	–	–	–	–	–	–	–	–	–	–	418	0	480	0	594	0	ps

Table 51: Input Slew Rate derating for NV-DDR2 differential (V_{CCQ} = 1.7–1.95V)

DQ V/ns	Δ^tDS, Δ^tDH Derating (ps) $V_{IH(AC)}/V_{IL(AC)}$= V_{REF} ±250mV, $V_{IH(DC)}/V_{IL(DC)}$ = V_{REF} ±125mV																Unit
	DQS_t/DQS_c Slew Rate																
	2 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1 V/ns		0.8 V/ns		0.6 V/ns		
	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	
2	0	0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ps
1.5	0	0	7	7	–	–	–	–	–	–	–	–	–	–	–	–	ps
1	0	0	7	7	16	16	–	–	–	–	–	–	–	–	–	–	ps
0.9	14	14	21	21	30	30	41	41	–	–	–	–	–	–	–	–	ps
0.8	31	31	38	38	47	47	58	58	73	73	–	–	–	–	–	–	ps
0.7	–	–	61	61	69	69	80	80	90	90	116	116	–	–	–	–	ps
0.6	–	–	–	–	99	99	100	100	100	100	100	100	100	100	–	–	ps
0.5	–	–	–	–	–	–	150	150	150	150	150	150	150	150	150	150	ps
0.4	–	–	–	–	–	–	–	–	200	200	200	200	200	200	200	200	ps
0.3	–	–	–	–	–	–	–	–	–	–	225	225	225	225	225	225	ps

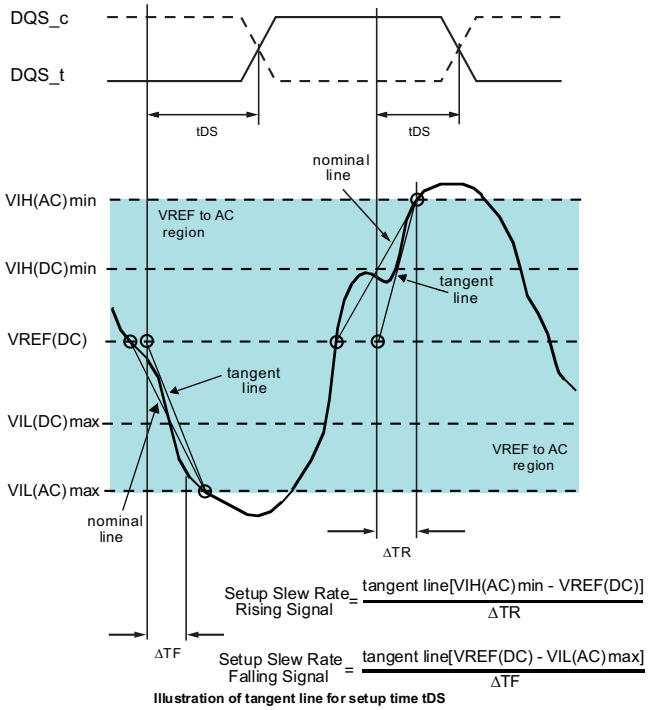
Figure 86: Nominal Slew Rate for Data Setup Time (^{t}DS), NV-DDR2 only



$$\text{Setup Slew Rate Falling Signal} = \frac{\text{VREF(DC)} - \text{VIL(AC)max}}{\Delta TF} \qquad \text{Setup Slew Rate Rising Signal} = \frac{\text{VIL(AC)min} - \text{VREF(DC)}}{\Delta TR}$$

Illustration of nominal slew rate for setup time tDS

Figure 87: Tangent Line for Data Setup Time (^{t}DS), NV-DDR2 only



$$\text{Setup Slew Rate Rising Signal} = \frac{\text{tangent line[VIH(AC)min} - \text{VREF(DC)]}}{\Delta TR}$$

$$\text{Setup Slew Rate Falling Signal} = \frac{\text{tangent line[VREF(DC)} - \text{VIL(AC)max]}}{\Delta TF}$$

Illustration of tangent line for setup time tDS

Figure 88: Nominal Slew Rate for Data Hold Time (^{t}DH), NV-DDR2 only

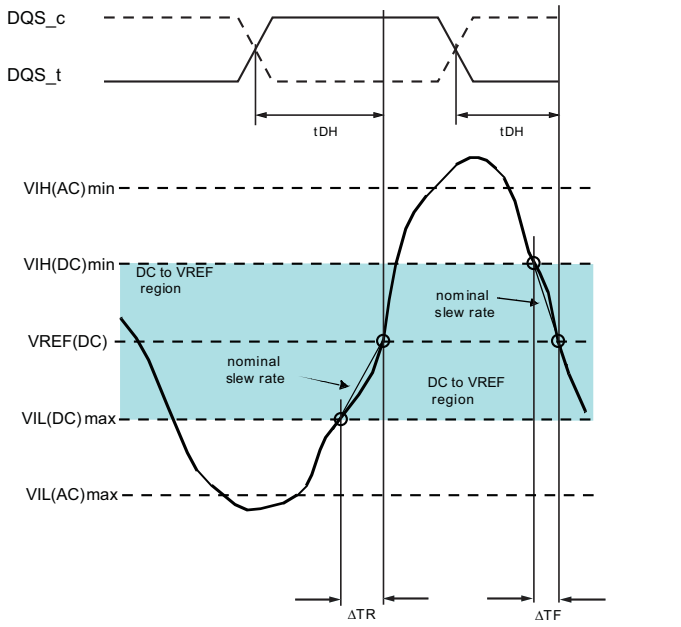


Illustration of nominal slew rate for hold time tDH

Figure 89: Tangent Line for Data Hold Time (^{t}DS), NV-DDR2 only

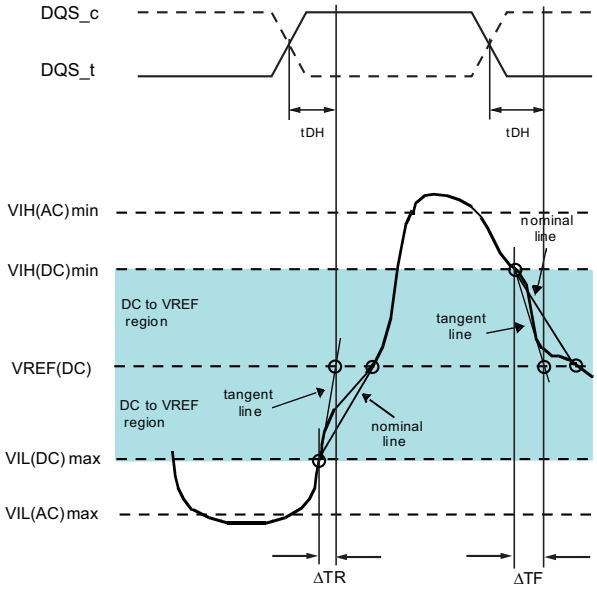


Illustration of tangent line for for hold time tDH

Output Slew Rate

The output slew rate is tested using the following setup with only one die per DQ channel.

Table 52: Test Conditions for Output Slew Rate

Parameter	Asynchronous/NV-DDR Interface[1]	NV-DDR2 single-ended[1]	NV-DDR2 differential[1]
$V_{OL(DC)}$	0.4 x V_{CCQ}	–	–
$V_{OH(DC)}$	0.6 x V_{CCQ}	–	–
$V_{OL(AC)}$[2]	0.3 x V_{CCQ}	V_{TT} - (V_{CCQ} * 0.10)	–
$V_{OH(AC)}$[2]	0.7 x V_{CCQ}	V_{TT} + (V_{CCQ} * 0.10)	–
$V_{OLdiff(AC)}$	–	–	-0.2 * V_{CCQ}
$V_{OHdiff(AC)}$	–	–	0.2 * V_{CCQ}
Rising Edge (^{t}RISE)	$V_{OL(DC)}$ to $V_{OH(AC)}$	$V_{OL(AC)}$ to $V_{OH(AC)}$	–
Falling Edge (^{t}FALL)	$V_{OH(DC)}$ to $V_{OL(AC)}$	$V_{OH(AC)}$ to $V_{OL(AC)}$	–
Differential rising edge (^{t}RISEdiff)	–	–	$V_{OLdiff(AC)}$ to $V_{OHdiff(AC)}$
Differential falling edge (^{t}FALLdiff)	–	–	$V_{OHdiff(AC)}$ to $V_{OLdiff(AC)}$
Output slew rate rising edge	[$V_{OH(AC)}$ – $V_{OL(DC)}$] / ^{t}RISE	[$V_{OH(AC)}$ – $V_{OL(DC)}$] / ^{t}RISE	[$V_{OHdiff(AC)}$ – $V_{OLdiff(AC)}$] / ^{t}RISEdiff
Output slew rate falling edge	[$V_{OH(DC)}$ – $V_{OL(AC)}$] / ^{t}FALL	[$V_{OH(AC)}$ – $V_{OL(AC)}$] / ^{t}FALL	[$V_{OHdiff(AC)}$ – $V_{OLdiff(AC)}$] / ^{t}FALLdiff
Output reference load[2]	5pf to V_{SS}	5pf to V_{SS}	5pf to V_{SS}
Temperature Range	T_{OPER}	T_{OPER}	T_{OPER}

Notes: 1. 1.8V V_{CCQ} is required for asynchronous, NV-DDR, and NV-DDR2 operations.
2. V_{TT} is 0.5 x V_{CCQ}.

Table 53: Output Slew Rate for Single-Ended Asynchronous, NV-DDR or NV-DDR2 (V_{CCQ} = 1.7–1.95V)

Output Drive Strength	Min	Max	Unit
25 Ohms	0.85	5	V/ns
35 Ohms	0.75	4	V/ns
50 Ohms	0.6	4	V/ns

Table 54: Output Slew Rate for NV-DDR2 differential (V_{CCQ} = 1.7–1.95V)

Output Drive Strength	Min	Max	Unit
25 Ohms	1.7	10.0	V/ns
35 Ohms	1.5	8.0	V/ns
50 Ohms	1.2	8.0	V/ns

Table 55: Output Slew Rate Matching Ratio for NV-DDR2

Drive Strength	Minimum	Maximum
Output Slew Rate matching ratio (pull-up to pull-down)	0.7	1.4

Notes: 1. The output slew rate mismatch is determined by the ratio of fast slew rate and slow slew rate. If the rising edge is faster than the falling edge, then divide the rising slew rate by the falling slew rate. If the failing edge is faster than the rising edge, then divide the falling slew rate by the rising slew rate.
2. The output slew rate mismatch is verified by design and characterization; it may not be subject to production testing.

Slew rates are measured under normal SSO conditions, with half of the DQ signals per data byte driving high and half of the DQ signals per data byte driving low. The output slew rate is measured per individual DQ signal.

Power Cycle Requirements

Upon power-down the NAND device requires a maximum voltage and minimum time that the host must hold V_{CC} and V_{CCQ} below the voltage prior to power-on.

Table 56: Power Cycle Requirements

Parameter	Value	Unit
Maximum V_{CC}/V_{CCQ}	100	mV
Minimum time below maximum voltage	100	ns

The NAND device will successfully power-up over the range of V_{CC}/V_{CCQ} slew rates for the following range:

Power supply voltage = 3.3V/35ms: 0.094 mV/µs to 100 mV/µs

Power supply voltage = 1.8V/25ms: 0.072 mV/µs to 100 mV/µs

Electrical Characteristics

Stresses greater than those listed can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods can affect reliability.

Table 57: Absolute Maximum Ratings by Device

Parameter	Symbol	Min[1]	Max[1]	Unit
Voltage input	V_{IN}	-0.45	2.4	V
V_{CC} supply voltage	V_{CC}	-0.6	4.6	V
V_{CCQ} supply voltage	V_{CCQ}	-0.45	2.4	V
V_{REFQ} supply voltage	V_{REFQ}	-0.45	2.4	V
Storage temperature	T_{STG}	-65	150	°C

Notes: 1. Voltage on any pin relative to V_{SS}.

Table 58: Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Operating temperature	T_{OPER}	0	70	°C
V_{CC} supply voltage	V_{CC}	2.7	3.6	V
V_{CCQ} supply voltage	V_{CCQ}	1.7	1.95	V
V_{REFQ} supply voltage	V_{REFQ}	0.49 x V_{CCQ}	0.51 x V_{CCQ}	V
V_{SS} ground voltage	V_{SS}	0	0	V

Notes: 1. Operating temperature (T_{OPER}) is the case surface temperature on the center/top of the NAND.
2. AC Noise on the supply voltages shall not exceed ±3% (10 kHz to 800 MHz). AC and DC noise together shall stay within the Min-Max range specified in this table.

Table 59: Valid Blocks per LUN

Parameter	Symbol	Min	Max	Unit	Notes
FxxL05Bxxxxxxxxxxx-AF	NVB	2094	2192	Blocks	1
FxxL05Bxxxxxxxxxxx-AR		TBD			

Notes: 1. Invalid blocks are blocks that contain one or more bad bits beyond ECC. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; however, the total number of available blocks will not drop below NVB during the endurance life of the device. Do not erase or program blocks marked invalid from the factory.

Package Electrical Specification and Pad Capacitance

The requirements in this section are optional for the Asynchronous, NV-DDR, and NV-DDR2 interfaces. The requirements in this section are optional for the NV-DDR2 interface when the device supports I/O speeds 533 MT/s or less and required for NV-DDR2 interface when the device supports I/O speeds greater than 533 MT/s.

Z_{IO} applies to DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c. $Td_{IO\ RE}$ applies to RE_t and RE_c. Z_{IO} and $Td_{IO\ Mismatch}$ apply to DQ[7:0], DQS_t, and DQS_c. Mismatch and Delta values are required to be met across same data bus on given package (for example, package channel), but not required across all channels on a given package. All other pins only need meet requirements in on page.

Table 60: Capacitance: 132-Ball BGA Package

Description	Symbol	<400 MT/s		533 MT/s		Unit	Notes
		Min	Max	Min	Max		
Input/Output ZPKG	Z_{IO}	35	90	35	90	Ohms	1
Delta Z_{PKG} for DQS_t and DQS_c	$DZ_{IO\ DQS}$	–	10	–	10	Ohms	7
Input/Output package delay	Td_{IO}	–	160	–	160	ps	1
Input/Output package delay	$Td_{IO\ RE}$	–	160	–	160	ps	
Input/Output package delay mismatch	$Td_{IO\ Mismatch}$	–	50	–	40	ps	5
Delta package delay for DQS_t and DQS_c	$DTd_{IO\ DQS}$	–	10	–	10	ps	
Delta Z_{PKG} for RE_t and RE_c	$DZ_{IO\ RE}$	–	10	–	10	Ohms	
Delta package delay for RE_t and RE_c	$DTd_{IO\ RE}$	–	10	–	10	ps	

Notes:
1. Z_{IO} and Td_{IO} apply to DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c. All other pins only need meet ONFI 3.0 requirements.
2. Test conditions: T_{OPER} = 25ºC, f = 100MHz, V_{IN} = 0V.
3. Verified in device characterization; not 100% tested. The package parasitic (L and C) are validated using package only samples. The capacitance is measured with V_{CC}, V_{CCQ}, V_{SS}, V_{SSQ} shorted with all other signal pins floating. The inductance is measured with V_{CC}, V_{CCQ}, V_{SS}, and V_{SSQ} shorted and all other signal pins shorted at the die side (not pin).
4. Package only impedance (Z_{PKG}) is calculated based on the L_{PKG} and C_{PKG} total for a given pin where: Z_{PKG} (total per pin) = SQRT(L_{PKG}/C_{PKG}).
5. Mismatch for Td_{IO} ($Td_{IO\ Mismatch}$) is calculated based on L_{PKG} and C_{PKG} total for a given pin where: Td_{PKG}(total per pin) = SQRT(L_{PKG} × C_{PKG}).
6. Package only delay (T_{PKG}) is calculated based on L_{PKG} and C_{PKG} total for a given pin where: Td_{PKG} (total per pin) = S_{QRT}(L_{PKG} × C_{PKG}).
7. Delta for DQS is Absolute value of Z_{IO}(DQS_t - Z_{IO}(DQS_c)) for impedance (Z) or absolute value of Td_{IO}(DQS_t) - Td_{IO}(DQS_c) for delay (Td).
8. Delta for RE is absolute value of Z_{IO}(RE_t - Z_{IO}(RE_c)) for impedance (Z) or absolute value of Td_{IO}(RE_t) - Td_{IO}(RE_c) for delay (Td).

Table 61: LUN Pad Specifications

Description	Symbol	<400 MT/s		533 MT/s		Unit	Notes
		Min	Max	Min	Max		
Input/Output pad capacitance	C_Pad_{IO}	–	1.6	–	1.6	pF	1
Delta input/output pad capacitance for DQS_t and DQS_c	$D\_C\_Pad_{IO\ DQS}$	0	0.2	0	0.2	pF	4
Delta input/output pad capacitance for RE_t and RE_c	$D\_C\_Pad_{IO\ RE}$	0	0.2	0	0.2	pF	3

Notes:
1. LUN Pad capacitances apply to DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c. All other LUN pads only need to meet ONFI legacy capacitance requirements.
2. Verified in device characterization; not 100% tested. These parameters are not subject to a production test. They are verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with V_{CC}, V_{CCQ}, V_{SS}, and V_{SSQ} applied and all other pins floating (except the pin under test). V_{CCQ} = 1.2V, VBIAS = V_{CCQ}/2 and on-die termination off.
3. These parameters apply to monolithic LUN, obtained by de-embedding the package L and C parasitics.
4. Delta for DQS is absolute value of C_PAD_{IO}(DQS_t) - C_PAD_{IO}(DQS_c).
5. Delta for RE is absolute value of C_PAD_{IO}(RE_t) - C_PAD_{IO}(RE_c).

Table 62: Test Conditions

Parameter	Asynchronous and NV-DDR	NV-DDR2 single-ended	NV-DDR2 differential	Notes
Rising input transition	$V_{IL(DC)}$ to $V_{IH(AC)}$	$V_{IL(DC)}$ to $V_{IH(AC)}$	$V_{ILdiff(DC)}$ max to $V_{IHdiff(AC)}$ min	1
Falling input transition	$V_{IH(DC)}$ to $V_{IL(AC)}$	$V_{IH(DC)}$ to $V_{IL(AC)}$	$V_{IHdiff(DC)}$ max to $V_{ILdiff(AC)}$ min	1
Input rise and fall slew rates	1 V/ns	1 V/ns	2 V/ns	–
Input timing levels	V_{CCQ}/2	V_{REFQ}	cross-point	–
Output timing levels	V_{CCQ}/2	V_{TT}	cross-point	
Output load: Nominal output drive strength	5pF to V_{SS}	5pF to V_{SS}	5pF to V_{SS}	2, 3, 4

Notes:
1. The receiver will effectively switch as a result of the signal crossing the AC input level; it will remain in that status as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.
2. Transmission line delay is assumed to be very small.
3. This test setup applies to all package configurations.
4. V_{TT} is 0.5 x V_{CCQ}.

Electrical Specifications – DC Characteristics and Operating Conditions (Asynchronous)

Table 63: DC Characteristics and Operating Characteristics (Asynchronous Interface)

Parameter	Conditions	Symbol	Min[1]	Max[1]	Unit
Array read current (active)	–	I_{CC1_A}	–	55	mA
	–	I_{CCQ1_A}	–	5	
Array program current (active)	–	I_{CC2_A}	–	55	mA
	–	I_{CCQ2_A}	–	8	
Erase current (active)	–	I_{CC3_A}	–	55	mA
	–	I_{CCQ3_A}	–	5	
I/O burst read current	$^{t}RC = {}^{t}RC$ (MIN); I_{OUT} = 0mA	I_{CC4R_A}	–	10	mA
		I_{CCQ4R_A}	–	7	
I/O burst write current	$^{t}WC = {}^{t}WC$ (MIN)	I_{CC4W_A}	–	12	mA
		I_{CCQ4W_A}	–	6	
Bus idle current	–	I_{CC5_A}	–	7	mA
	–	I_{CCQ5_A}	–	7	
Current during first RESET command after power-on	–	I_{CC6}	–	36	mA
Power-up peak current (V_{CC})	–	$I_{CC\_Peak\_Up}$		20	mA
Power-up peak current (V_{CCQ})	–	$I_{CC\_Peak\_Down}$		20	mA
Power-up peak current (V_{CCQ})	–	$I_{CCQ\_Peak\_Up}$		10	mA
Power-down peak current (V_{CCQ})	–	$I_{CCQ\_Peak\_Down}$		15	mA
Standby current - V_{CC}	CE# = V_{CCQ} - 0.2V; WP# = 0V/V_{CCQ}	I_{SB}	–	350	µA
Standby current - V_{CCQ}	CE# = V_{CCQ} - 0.2V; WP# = 0V/V_{CCQ}	I_{SBQ}	–	300	µA
Staggered power-up current	$^{t}RISE$ = 1ms; C_{LINE} = 0.1uF	I_{ST}	–	10	mA

Notes:
1. All values are per die (LUN) unless specified otherwise.
2. During I_{SBQ} testing, DQS_t/DQS_c, RE_t/RE_c, and DQ[7:0] are floating.
3. During I_{CC} testing, on-die terminations (ODT) is not enabled.
4. The Design Datasheet should not be referenced for current values once a Advance (customer) datasheet version is released.
5. For the I_{CC_Peak} and I_{CCQ_Peak} currents the entire duration of the operation should be considered when calculating the maximum average current of the worst case 1µs subset of the operation.

Electrical Specifications – DC Characteristics and Operating Conditions (NV-DDR and NV-DDR2)

Table 64: DC Characteristics and Operating Characteristics (NV-DDR Interface) 1.8V V_{CCQ}

Parameter	Conditions	Symbol	Min[1]	Typ		Max[1]	Unit
				Single-plane	Two-plane		
Array read current (active)	CE# = V_{IL}; ^{t}CK = ^{t}CK (MIN) or ^{t}RC = ^{t}RC (MIN)	I_{CC1_S}	–	TBD	44.4	55	mA
		I_{CCQ1_S}	–	TBD	1.5	5	
Array program current (active)	^{t}CK = ^{t}CK (MIN) or ^{t}DSC = ^{t}DSC (MIN)	I_{CC2_S}	–	TBD	46.7	55	mA
		I_{CCQ2_S}	–	TBD	2	8	
Erase current (active)	^{t}CK = ^{t}CK (MIN)	I_{CC3_S}	–	TBD	50	55	mA
		I_{CCQ3_S}	–	TBD	1.5	5	
I/O burst read current	^{t}CK = ^{t}CK (MIN) or ^{t}RC = ^{t}RC (MIN); I_{OUT} = 0mA; ODT disabled	I_{CC4R_S}	–	9		12	mA
		I_{CCQ4R_S}	–	25		31	
I/O burst write current	^{t}CK = ^{t}CK (MIN) or ^{t}DSC= ^{t}DSC (MIN); ODT disabled	I_{CC4W_S}	–	12		15	mA
		I_{CCQ4W_S}	–	13		16	
Bus idle current	^{t}CK = ^{t}CK (MIN) NV-DDR	I_{CC5_S}	–	5		10	mA
		I_{CCQ5_S}	–	5		7	
Power-up peak current (V_{CC})	–	$I_{CC\_Peak\_Up}$	–	–		20	mA
Power-up peak current (V_{CCQ})	–	$I_{CC\_Peak\_Down}$	–	–		10	mA
Power-down peak current (V_{CC})	–	$I_{CCQ\_Peak\_Up}$	–	–		20	mA
Power-down peak current (V_{CCQ})	–	$I_{CCQ\_Peak\_Down}$	–	–		15	mA
Standby current - V_{CC}	CE# = V_{CCQ} - 0.2V; WP# = 0V/V_{CCQ}	I_{SB}	–	15		350	µA
Standby current - V_{CCQ}	CE# = V_{CCQ} - 0.2V; WP# = 0V/V_{CCQ}	I_{SBQ}	–	5		300	µA

Notes:
1. All values are per die (LUN) unless specified otherwise.
2. During I_{SBQ} testing, DQS_t/DQS_c, RE_t/RE_c, and DQ[7:0] are floating.
3. I_{CCQ1} only occurs for the first 20µs of a read command and I_{CCQ2} last 20µs of a program command.
4. During I_{CC} testing, on-die terminations (ODT) is not enabled.

Table 65: DC Characteristics and Operating Characteristics (NV-DDR2 Interface) 1.8V V_{CCQ}

Parameter	Conditions	Symbol	Min[1]	Typ		Max[1]	Unit	Notes
				Single-plane	Two-plane			
Array read current (active)	CE# = V_{IL}; ^{t}CK = ^{t}CK (MIN) or ^{t}RC = ^{t}RC (MIN)	I_{CC1_S}	–	TBD	44.4	55	mA	
		I_{CCQ1_S}	–	TBD	1.5	5		
Array program current (active)	^{t}CK = ^{t}CK (MIN) or ^{t}DSC = ^{t}DSC (MIN)	I_{CC2_S}	–	TBD	46.7	55	mA	
		I_{CCQ2_S}	–	TBD	2	8		

Table 65: DC Characteristics and Operating Characteristics (NV-DDR2 Interface) 1.8V V_{CCQ}

Parameter	Conditions	Symbol	Min[1]	Typ		Max[1]	Unit	Notes
				Single-plane	Two-plane			
Erase current (active)	$^{t}CK = {}^{t}CK$ (MIN)	I_{CC3_S}	–	TBD	50	55	mA	
		I_{CCQ3_S}	–	TBD	1.5	5		
I/O burst read current	$^{t}CK = {}^{t}CK$ (MIN) or $^{t}RC = {}^{t}RC$ (MIN); I_{OUT} = 0mA; ODT disabled	I_{CC4R_S}	–	6		8	mA	3
				13		16		4
				17		21		5
		I_{CCQ4R_S}	–	25		31	mA	3
				40		50		4
				65		81		5
I/O burst write current	$^{t}CK = {}^{t}CK$ (MIN) or $^{t}DSC = {}^{t}DSC$ (MIN); ODT disabled	I_{CC4W_S}	–	7		9	mA	3
				14		17		4
				18		22		5
		I_{CCQ4W_S}	–	13		16	mA	3
				25		32		4
				34		43		5
Bus idle current	$^{t}CK = {}^{t}CK$ (MIN) NV-DDR	I_{CC5_S}	–	5		7	mA	
		I_{CCQ5_S}	–	5		7		
Power-up peak current (V_{CC})	–	$I_{CC\_Peak\_Up}$	–	–		20	mA	
Power-up peak current (V_{CCQ})	–	$I_{CC\_Peak\_Down}$	–	–		10	mA	
Power-down peak current (V_{CC})	–	$I_{CCQ\_Peak\_Up}$	–	–		20	mA	
Power-down peak current (V_{CCQ})	–	$I_{CCQ\_Peak\_Down}$	–	–		15	mA	
Standby current - V_{CC}	CE# = V_{CCQ} - 0.2V; WP# = 0V/V_{CCQ}	I_{SB}	–	15		350	µA	
Standby current - V_{CCQ}	CE# = V_{CCQ} - 0.2V; WP# = 0V/V_{CCQ}	I_{SBQ}	–	5		300	µA	

Notes:
1. All values are per die (LUN) unless specified otherwise.
2. During I_{SBQ} testing, DQS_t/DQS_c, RE_t/RE_c, and DQ[7:0] are floating.
3. For speeds up to 200 MT/s.
4. For speeds greater than 200 MT/s up to 400 MT/s.
5. For speeds greater than 400 MT/s.
6. I_{CCQ1} only occurs for the first 20µs of a read command and I_{CCQ2} last 20µs of a program command.
7. During I_{CC} testing, on-die terminations (ODT) is not enabled.

Electrical Specifications – DC Characteristics and Operating Conditions (V_{CCQ})

Table 66: Asynchronous/NV-DDR DC Characteristics and Operating Characteristics (1.8V V_{CCQ})

Parameter	Condition	Symbol	Min	Max	Unit	Notes
AC input high voltage	CE#, DQ[7:0], DQS, ALE, CLE, CLK (WE#), W/R# (RE#), WP#	$V_{IH\ (AC)}$	0.8 × V_{CCQ}	See note	V	1
AC input low voltage		$V_{IL\ (AC)}$	See note	0.2 × V_{CCQ}	V	
DC input high voltage	DQ[7:0], DQS, ALE, CLE, CLK (WE#), W/R# (RE#)	$V_{IH\ (DC)}$	0.7 × V_{CCQ}	V_{CCQ} + 0.3	V	
DC input low voltage		$V_{IL\ (DC)}$	–0.3	0.3 × V_{CCQ}	V	
Input leakage current	Any input V_{IN} = 0V to V_{CCQ}	I_{LI}	–	±10	µA	2
Output leakage current	DQs are disabled; V_{OUT} = V_{CCQ}	I_{LO_pd}	–	1	µA	4
	DQs are disabled; V_{OUT} = 0V	I_{LO_pu}	–	5	µA	
Output low current (R/B#)	V_{OL} = 0.2V	I_{OL} (R/B#)	3	–	mA	3

Notes:
1. See AC Overshoot and Undershoot requirements.
2. All leakage currents are per LUN. For example, if a die (LUN) had a leakage current of ±10µA that would mean two die (LUNs) have a maximum leakage of ±20µA and four die (LUNs) have a maximum leakage current of ±40µA.
3. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full strength. See Feature Address 81h: Programmable R/B# Pull-Down Strength for additional details.
4. Absolute leakage value per I/O per NAND die (DQ[7:0], DQS_t, DQS_c, RE_t, RE_c).

Table 67: NV-DDR2 DC Characteristics and Operating Characteristics for Single-Ended signal (1.8V V_{CCQ})

Parameter	Condition	Symbol	Min	Max	Unit	Notes
AC input high voltage	DQ[7:0], DQS, ALE, CLE, WE#, RE#	$V_{IH(AC)}$	V_{REFQ} + 0.250	See note	V	4
AC input low voltage		$V_{IL(AC)}$	See note	V_{REFQ} - 0.250	V	4
AC input high voltage	CE#, WP#	$V_{IH(AC)}$	0.8 × V_{CCQ}	See note	V	4
AC input low voltage		$V_{IL(AC)}$	See note	0.2 × V_{CCQ}	V	4
DC input high voltage	DQ[7:0], DQS, ALE, CLE, WE#, RE#	$V_{IH(DC)}$	V_{REFQ} + 0.125	V_{CCQ} + 0.3	V	2
DC input low voltage		$V_{IL(DC)}$	-0.3	V_{REFQ} - 0.125	V	2
DC input high voltage	CE#, WP#	$V_{IH(DC)}$	0.7 × V_{CCQ}	V_{CCQ} + 0.3	V	
DC input low voltage		$V_{IL(DC)}$	–0.3	0.3 × V_{CCQ}	V	
Input leakage current	Any input V_{IN} = 0V to V_{CCQ}	I_{LI}	–	±10	µA	1
Output leakage current	DQ are disabled; V_{OUT} = V_{CCQ}	I_{LO_pd}	–	1	µA	5
	DQ are disabled; V_{OUT} = 0V	I_{LO_pu}	–	5		
Output low current (R/B#)	V_{OL} = 0.2V	I_{OL} (R/B#)	3	–	mA	3

Table 67: NV-DDR2 DC Characteristics and Operating Characteristics for Single-Ended signal (1.8V V_{CCQ})

Parameter	Condition	Symbol	Min	Max	Unit	Notes
V_{REFQ} leakage current	$V_{REFQ} = V_{CCQ}/2$ (all other pins not under test = 0V)	I_{VREFQ}	–	±5	µA	

Notes:
1. All leakage currents are per die (LUN). For example, two die (LUNs) have a maximum leakage current of ±20µA and four die (LUNs) have a maximum leakage current of ±40µA.
2. These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [$V_{IH(DC)}$ MAX, $V_{IL(DC)}$ MIN] for single-ended signals as well as the limitations for overshoot and undershoot.
3. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to "Full."
4. See AC Overshoot and Undershoot requirements.
5. Absolute leakage value per I/O per NAND die (DQ[7:0], DQS_t, DQS_c, RE_t, RE_c).

Table 68: NV-DDR2 DC Characteristics and Operating Characteristics for Differential signals (1.8V V_{CCQ})

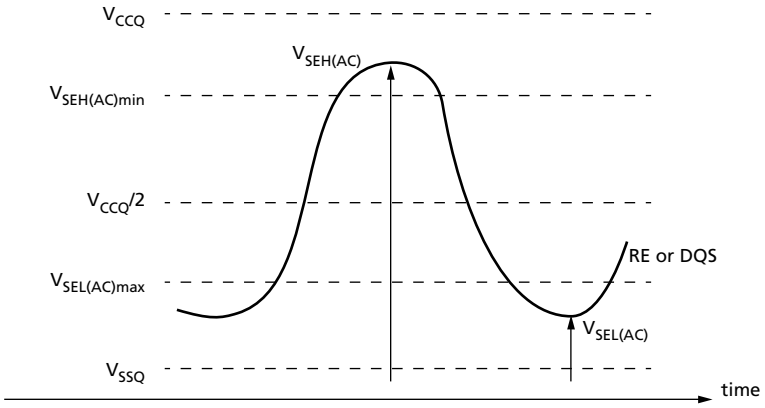
Parameter	Condition	Symbol	Min	Max	Unit	Notes
Differential AC input high voltage	DQS_t, DQS_c, RE_t, RE_c	$V_{IHdff(AC)}$	2 x [$V_{IH(DC)}$ - V_{REF}]	see note	V	2
Differential AC input low voltage		$V_{ILdff(AC)}$	see note	2 x [V_{REF} - $V_{IL(AC)}$]	V	2
Differential DC input high voltage	DQS_t, DQS_c, RE_t, RE_c	$V_{IHdff(DC)}$	2 x [$V_{IH(DC)}$ - V_{REF}]	see note	V	2
Differential DC input low voltage		$V_{ILdff(DC)}$	see note	2 x [V_{REF} - $V_{IL(AC)}$]	V	2
Input leakage current	Any input V_{IN} = 0V to V_{CCQ}	I_{LI}	–	±10	µA	1
Output leakage current	DQ are disabled; $V_{OUT} = V_{CCQ}$	I_{LO_pd}	–	1	µA	4
	DQ are disabled; V_{OUT} = 0V	I_{LO_pu}	–	5	µA	
Output low current (R/B#)	V_{OL} = 0.2V	I_{LO} (R/B#)	3	–	mA	3
V_{REFQ} leakage current	$V_{REFQ} = V_{CCQ}/2$ (all other pins not under test = 0V)	I_{VREFQ}	–	±5	µA	

Notes:
1. All leakage currents are per die (LUN). For example, two die (LUNs) have a maximum leakage current of ±20µA and four die (LUNs) have a maximum leakage current of ±40µA.
2. These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [$V_{IH(DC)}$ MAX, $V_{IL(DC)}$ MIN] for single-ended signals as well as the limitations for overshoot and undershoot.
3. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to "Full."
4. Absolute leakage value per I/O per NAND die (DQ[7:0], DQS_t, DQS_c, RE_t, RE_c).

Single-Ended Requirements for Differential signals

Each individual component of a differential signal (RE_t, RE_c, DQS_t, or DQS_c) shall comply with requirements for single-ended signals. RE_t and RE_c shall meet $V_{SEH(AC)}$ Min / $V_{SEL(AC)}$ Max in every half-cycle. DQS_t and DQS_c shall meet $V_{SEH(AC)}$ Min / $V_{SEL(AC)}$ Max in every half-cycle preceding and following a valid transition.

Figure 90: Single-Ended requirements for Differential Signals



While control (e.g., ALE, CLE) and DQ signal requirements are with respect to V_{REFQ}, the single-ended components of differential signals have a requirement with respect to $V_{CCQ}/2$; this is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach $V_{SEL(AC)}$ Max, $V_{SEH(AC)}$ Min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table 69: Single-Ended Levels for RE_t, RE_c, DQS_t, DQS_c (1.8V V_{CCQ})

Parameter	Symbol	Min	Max	Unit	Notes
Single-Ended high level	$V_{SEH(AC)}$	$V_{CCQ}/2$ + 0.250	see note	V	1
Single-Ended low level	$V_{SEL(AC)}$	see note	$V_{CCQ}/2$ - 0.250	V	1

Notes: 1. These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [$V_{IH(DC)}$ Max, $V_{IL(DC)}$ Min] for single-ended signals as well as the limitations for overshoot and undershoot.

Table 70: Differential AC Input/Output Parameters

Parameter	Symbol	Min	Max	Unit	Notes
AC differential input cross-point voltage relative to $V_{CCQ}/2$	$V_{IX(AC)}$	0.5 x V_{CCQ} - 0.175	0.5 x V_{CCQ} + 0.175	V	1
AC differential output cross-point voltage	$V_{OX(AC)}$	0.5 x V_{CCQ} - 0.2	0.5 x V_{CCQ} + 0.2	V	2, 3, 4

Notes: 1. The typical value of $V_{IX(AC)}$ is expected to be 0.5 x V_{CCQ} of the transmitting device. $V_{IX(AC)}$ is expected to track variations in V_{CCQ}. $V_{IX(AC)}$ indicates the voltage at which differential input signals shall cross.
2. The typical value of $V_{OX(AC)}$ is expected to be 0.5 x V_{CCQ} of the transmitting device. $V_{OX(AC)}$ is expected to track variations in V_{CCQ}. $V_{OX(AC)}$ indicates the voltage at which differential input signals shall cross.
3. $V_{OX(AC)}$ is measured with ½ DQ signals per data byte driving logic HIGH and ½ DQ signals per data byte driving logic LOW.

4. $V_{OX(AC)}$ is verified by design and characterization; it may not be subject to production testing.

Electrical Specifications – AC Characteristics and Operating Conditions (Asynchronous)

Table 71: AC Characteristics: Asynchronous Command, Address, and Data

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock Period		100		50		35		30		25		20		ns	
Frequency		≈10		≈20		≈28		≈33		≈40		~50		MHz	
ALE to data start	^{t}ADL	150	–	150	–	150	–	150	–	150	–	150	–	ns	1
ALE hold time	^{t}ALH	20	–	10	–	10	–	5	–	5	–	5	–	ns	
ALE setup time	^{t}ALS	50	–	25	–	15	–	10	–	10	–	10	–	ns	
ALE to RE# delay	^{t}AR	25	–	10	–	10	–	10	–	10	–	10	–	ns	
CE# access time	^{t}CEA	–	100	–	45	–	30	–	25	–	25	–	25	ns	
CE# HIGH hold time prior to VOLUME SELECT (E1h)	^{t}CEH	20	–	20	–	20	–	20	–	20	–	20	–	ns	
CE# hold time	^{t}CH	20	–	10	–	10	–	5	–	5	–	5	–	ns	
Delay before CE# HIGH for any Volume after a Volume is selected	^{t}CEVDLY	50	–	50	–	50	–	50	–	50	–	50	–	ns	
CE# high to output high-Z	^{t}CHZ	–	100	–	50	–	50	–	50	–	30	–	30	ns	2
CLE hold time	^{t}CLH	20	–	10	–	10	–	5	–	5	–	5	–	ns	
CLE to RE# delay	^{t}CLR	20	–	10	–	10	–	10	–	10	–	10	–	ns	
CLE setup time	^{t}CLS	50	–	25	–	15	–	10	–	10	–	10	–	ns	
CE# high to output hold	^{t}COH	0	–	15	–	15	–	15	–	15	–	15	–	ns	
CE# setup time	^{t}CS	70	–	35	–	25	–	25	–	20	–	15	–	ns	
CE# to RE# LOW or RE_t/RE_c	^{t}CR	10	–	10	–	10	–	10	–	10	–	10	–	ns	
CE# to RE# LOW after CE# has been HIGH for >1µs	^{t}CR2	100	–	100	–	100	–	100	–	100	–	100	–	ns	
	^{t}CR2 (Read ID)	150	–	150	–	150	–	150	–	150	–	150	–	ns	
CE# setup time for data input after CE# has been HIGH for >1µs	^{t}CS3	100	–	100	–	100	–	100	–	100	–	100	–	ns	
Data hold time	^{t}DH	20	–	10	–	5	–	5	–	5	–	5	–	ns	
Data setup time	^{t}DS	40	–	20	–	15	–	10	–	10	–	7	–	ns	
Eni LOW until any issued command is ignored	^{t}ENi	–	15	–	15	–	15	–	15	–	15	–	15	ns	

Table 71: AC Characteristics: Asynchronous Command, Address, and Data (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CE_# LOW until ENo LOW	tENo	–	50	–	50	–	50	–	50	–	50	–	50	ns	
Output high-Z to RE# low	tIR	10	–	0	–	0	–	0	–	0	–	0	–	ns	
RE# cycle time	tRC	100	–	50	–	35	–	30	–	25	–	20	–	ns	
RE# access time	tREA	–	40	–	30	–	25	–	20	–	20	–	16	ns	3
RE# high hold time	tREH	30	–	15	–	15	–	10	–	10	–	7	–	ns	3
RE# high to output hold	tRHOH	0	–	15	–	15	–	15	–	15	–	15	–	ns	3
RE# high to WE# low	tRHW	200	–	100	–	100	–	100	–	100	–	100	–	ns	
RE# high to output high-Z	tRHZ	–	200	–	100	–	100	–	100	–	100	–	100	ns	2, 3
RE# low to output hold	tRLOH	0	–	0	–	0	–	0	–	5	–	5	–	ns	3
RE# pulse width	tRP	50	–	25	–	17	–	15	–	12	–	10	–	ns	
Ready to RE# low	tRR	40	–	20	–	20	–	20	–	20	–	20	–	ns	
WE# high to R/B# low	tWB	–	200	–	100	–	100	–	100	–	100	–	100	ns	4
WE# cycle time	tWC	100	–	45	–	35	–	30	–	25	–	20	–	ns	
WE# high hold time	tWH	30	–	15	–	15	–	10	–	10	–	7	–	ns	
WE# high to RE# low	tWHR	120	–	80	–	80	–	60	–	60	–	60	–	ns	
WE# pulse width	tWP	50	–	25	–	17	–	15	–	12	–	10	–	ns	
WP# transition to WE# low	tWW	100	–	100	–	100	–	100	–	100	–	100	–	ns	
Delay before next command after a Volume is selected	tVDLY	50	–	50	–	50	–	50	–	50	–	50	–	ns	

Notes:
1. Timing for tADL begins in the address cycle, on the final rising edge of WE# and ends with the first rising edge of WE# for data input. tADL SPEC for SET FEATURES operations is 70ns.
2. Data transition is measured ±200mV from steady-steady voltage with load. This parameter is sampled and not 100 percent tested.
3. AC characteristics may need to be relaxed if output drive strength is not set to at least nominal.
4. Any command (including read status commands) cannot be issued during tWB, even if R/B# or RDY is ready.
5. tCR2 (MIN) is 150ns for read ID sequence only. For all other command sequences tCR2 (MIN) requirement is 100ns.

Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR and NV-DDR2)

Table 72: AC Characteristics: NV-DDR Command, Address, and Data

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock Period		50		30		20		15		12		10		ns	
Frequency		≈20		≈33		≈50		≈67		≈83		≈100		MHz	
Access window of DQ[7:0] from CLK	^{t}AC	3	20	3	20	3	20	3	20	3	20	3	20	ns	
ALE to data loading time	^{t}ADL	150	–	150	–	150	–	150	–	150	–	150	–	ns	6
Cmd, Addr, Data delay	^{t}CAD	25	–	25	–	25	–	25	–	25	–	25	–	ns	1
ALE, CLE, W/R# hold	^{t}CALH	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
ALE, CLE, W/R# setup	^{t}CALS	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
DQ hold - Cmd, Addr	^{t}CAH	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
DQ setup - Cmd, Addr	^{t}CAS	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
CE# hold	^{t}CH	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
CE# HIGH hold time prior to VOLUME SELECT (E1h)	^{t}CEH	20	–	20	–	20	–	20	–	20	–	20	–	ns	
Delay before CE# HIGH for any Volume after a Volume is selected	^{t}CEVDLY	50	–	50	–	50	–	50	–	50	–	50	–	ns	
Average CLK cycle time	^{t}CK (avg)	50	100	30	50	20	30	15	20	12	15	10	12	ns	2
Absolute CLK cycle time, from rising edge to rising edge	^{t}CK (abs)	^{t}CK(abs) MIN = ^{t}CK(avg) + ^{t}JIT(per) MIN ^{t}CK(abs) MAX = $^{\tau}$CK (avg) + ^{t}JIT(per) MAX												ns	
CLK cycle HIGH	^{t}CKH (abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	^{t}CK	3
CLK cycle LOW	^{t}CKL (abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	^{t}CK	3
Data output end to W/R# HIGH	^{t}CKWR	^{t}CKWR(MIN) = RoundUp[^{t}DQSCK(MAX) + ^{t}CK) / ^{t}CK]												^{t}CK	
CE# setup time for data input and data output after CE# has been HIGH for >1µs	^{t}CS3	75	–	75	–	75	–	75	–	75	–	75	–	ns	
CE# setup	^{t}CS	35	–	25	–	15	–	15	–	15	–	15	–	ns	
Data In hold	^{t}DH	5	–	2.5	–	1.7	–	1.3	–	1.1	–	0.9	–	ns	

Table 72: AC Characteristics: NV-DDR Command, Address, and Data

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access window of DQS from CLK	^{t}DQSCK	–	20	–	20	–	20	–	20	–	20	–	20	ns	
DQS, DQ[7:0] Driven by NAND	^{t}DQSD	–	18	–	18	–	18	–	18	–	18	–	18	ns	
DQS, DQ[7:0] to tri-state	^{t}DQSHZ	–	20	–	20	–	20	–	20	–	20	–	20	ns	4
DQS input high pulse width	^{t}DQSH	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	^{t}CK	
DQS input low pulse width	^{t}DQSL	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	^{t}CK	
DQS-DQ skew	^{t}DQSQ	–	5	–	2.5	–	1.7	–	1.3	–	1.0	–	0.85	ns	
Data input	^{t}DQSS	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	^{t}CK	
Data In setup	^{t}DS	5	–	3	–	2	–	1.5	–	1.1	–	0.9	–	ns	
DQS falling edge from CLK rising - hold	^{t}DSH	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	^{t}CK	
DQS falling to CLK rising - setup	^{t}DSS	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	^{t}CK	
Data Valid Window	^{t}DVW	^{t}DVW = ^{t}QH - ^{t}DQSQ												ns	
ENi LOW until any issued command is ignored	^{t}ENi	–	15	–	15	–	15	–	15	–	15	–	15	ns	
CE_# LOW until ENo LOW	^{t}ENo	–	50	–	50	–	50	–	50	–	50	–	50	ns	
Half Clock Period	^{t}HP	^{t}HP = Min(^{t}CKH, ^{t}CKL)												ns	
The deviation of a given ^{t}CK(abs) from ^{t}CK (avg)	^{t}JIT(per)	-0.7	0.7	-0.7	0.7	-0.7	0.7	-0.6	0.6	-0.6	0.6	-0.5	0.5	ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access	^{t}QH	^{t}QH = ^{t}HP - ^{t}QHS												ns	
Data Hold Skew Factor	^{t}QHS	–	6	–	3	–	2	–	1.5	–	1.2	–	1	ns	
Data output to command, address, or data input	^{t}RHW	100	–	100	–	100	–	100	–	100	–	100	–	ns	
Ready to data output	^{t}RR	20	–	20	–	20	–	20	–	20	–	20	–	ns	
CLK high to R/B# low	^{t}WB	–	100	–	100	–	100	–	100	–	100	–	100	ns	
Command cycle to data output	^{t}WHR	80	–	80	–	80	–	80	–	80	–	80	–	ns	
DQS write preamble	^{t}WPRE	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	^{t}CK	
DQS write postamble	^{t}WPST	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	^{t}CK	

Table 72: AC Characteristics: NV-DDR Command, Address, and Data

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
W/R# LOW to data output cycle	tWRCK	20	–	20	–	20	–	20	–	20	–	20	–	ns	
WP# transition to command cycle	tWW	100	–	100	–	100	–	100	–	100	–	100	–	ns	
Delay before next command after a volume is selected	tVDLY	50	–	50	–	50	–	50	–	50	–	50	–	ns	

Notes:
1. Delay is from start of command to next command, address, or data cycle; start of address to next command, address, or data cycle; and end of data to start of next command, address, or data cycle.
2. tCK(avg) is the average clock period over any consecutive 200-cycle window.
3. tCKH(abs) and tCKL(abs) include static offset and duty cycle jitter.
4. tDQSHZ begins when W/R# is latched HIGH by CLK. This parameter is not referenced to a specific voltage level; it specifies when the device outputs are no longer driving.
5. If RESET (FFh) is issued when the target is idle, the target goes busy for a maximum of 5µs.
6. tADL SPEC for SET FEATURES operations is 70ns.
7. Any command (including read status commands) cannot be issued during tWB, even if R/B# or RDY is ready.

Table 73: AC Characteristics: NV-DDR2 Command, Address, and Data for modes 0-4

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock Period		30		25		15		12		10		ns	
Frequency		≈33		≈40		≈66		≈83		≈100		MHz	
Command and Address													
Access window of DQ[7:0] from RE# LOW or RE_t/RE_c	tAC	3	25	3	25	3	25	3	25	3	25	ns	
ALE to data start	tADL	100	–	100	–	100	–	100	–	100	–	ns	13
ALE to RE# delay	tAR	10	–	10	–	10	–	10	–	10	–	ns	
DQ hold–command, address	tCAH	5	–	5	–	5	–	5	–	5	–	ns	
ALE, CLE hold	tCALH	5	–	5	–	5	–	5	–	5	–	ns	
ALE, CLE setup with ODT disabled	tCALS	15	–	15	–	15	–	15	–	15	–	ns	
ALE, CLE setup with ODT enabled	tCALS2	25	–	25	–	25	–	25	–	25	–	ns	
DQ setup–command, address	tCAS	5	–	5	–	5	–	5	–	5	–	ns	
CE# HIGH hold time prior to VOLUME SELECT (E1h)	tCEH	20	–	20	–	20	–	20	–	20	–	ns	
Delay before CE# HIGH for any Volume after a Volume is selected	tCEVDLY	50	–	50	–	50	–	50	–	50	–	ns	
CE# hold	tCH	5	–	5	–	5	–	5	–	5	–	ns	

Table 73: AC Characteristics: NV-DDR2 Command, Address, and Data for modes 0-4

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CE# high to output hi-Z	tCHZ	–	30	–	30	–	30	–	30	–	30	ns	1
CLE high to output hi-Z	tCLHZ	–	30	–	30	–	30	–	30	–	30	ns	1
CLE to RE# delay	tCLR	10	–	10	–	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c	tCR	10	–	10	–	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c if CE# has been HIGH for >1µs	tCR2	100	–	100	–	100	–	100	–	100	–	ns	
	tCR2 (Read ID)	150	–	150	–	150	–	150	–	150	–	ns	14
CE# setup time	tCS	20	–	20	–	20	–	20	–	20	–	ns	
CE# setup for data output with ODT disabled	tCS1	30	–	30	–	30	–	30	–	30	–	ns	
CE# setup for DQS/ DQ[7:0] with ODT enabled	tCS2	40	–	40	–	40	–	40	–	40	–	ns	17
CE# setup time to DQS (DQS_t) low after CE# has been HIGH for >1µs	tCD	100	–	100	–	100	–	100	–	100	–	ns	
ALE, CLE, WE#, hold time from CE# HIGH	tCSD	10	–	10	–	10	–	10	–	10	–	ns	
Eni LOW until any issued command is ignored	tENi	–	15	–	15	–	15	–	15	–	15	ns	
CE_# LOW until ENo LOW	tENo	–	50	–	50	–	50	–	50	–	50	ns	
Ready to RE# low	tRR	20	–	20	–	20	–	20	–	20	–	ns	
WE# high to R/B# low	tWB	–	100	–	100	–	100	–	100	–	100	ns	16
WE# cycle time	tWC	25	–	25	–	25	–	25	–	25	–	ns	
WE# high hold time	tWH	11	–	11	–	11	–	11	–	11	–	ns	
WE# high to RE# low	tWHR	80	–	80	–	80	–	80	–	80	–	ns	
WE# pulse width	tWP	11	–	11	–	11	–	11	–	11	–	ns	
WP# transition to WE# low	tWW	100	–	100	–	100	–	100	–	100	–	ns	
Delay before next command after a Volume is selected	tVDLY	50	–	50	–	50	–	50	–	50	–	ns	
Jitter													

Table 73: AC Characteristics: NV-DDR2 Command, Address, and Data for modes 0-4

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
The deviation of a given ^{t}DQS (abs)/ ^{t}DSC (abs) from a ^{t}DQS (avg)/^{t}DCS (avg)	^{t}JITper (DQS)	-2.4	2.4	-2.0	2.0	-1.2	1.2	-1.0	1.0	-0.8	0.8	ns	3, 5, 7
The deviation of a given ^{t}RC (abs)/^{t}DSC (abs) from a ^{t}RC (avg)/^{t}DCS (avg)	^{t}JITper (RE#)	-1.8	1.8	-1.5	1.5	-0.9	0.9	-0.75	0.75	-0.6	0.6	ns	3, 5, 7
Cycle to cycle jitter for DQS	^{t}JITcc (DQS)	4.8	–	4.0	–	2.4	–	2.0	–	1.6	–	ns	3, 6
Cycle to cycle jitter for RE#	^{t}JITcc (RE#)	3.6	–	3.0	–	1.8	–	1.5	–	1.2	–	ns	3, 6
Data Input													
DQS setup time for data input	^{t}CDQSS	30	–	30	–	30	–	30	–	30	–	ns	
DQS hold time for data input burst end	^{t}CDQSH	100	–	100	–	100	–	100	–	100	–	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE and CE# LOW during data burst	^{t}DBS	5	–	5	–	5	–	5	–	5	–	ns	
Data hold time	^{t}DH	4.0	–	3.3	–	2.0	–	1.1	–	0.7	–	ns	10
Data setup time	^{t}DS	4.0	–	3.3	–	2.0	–	1.1	–	0.7	–	ns	10
DQ input pulse width	^{t}DIPW	0.31	–	0.31	–	0.31	–	0.31	–	0.31	–	^{t}DQS (avg)	12
DQS input high pulse width	^{t}DQSH	0.43	–	0.43	–	0.43	–	0.43	–	0.43	–	^{t}DQS (avg)	
DQS input low pulse width	^{t}DQSL	0.43	–	0.43	–	0.43	–	0.43	–	0.43	–	^{t}DQS (avg)	
Average DQS cycle time	^{t}DSC (avg) or ^{t}DSC	30	–	25	–	15	–	12	–	10	–	ns	2
Absolute DQS cycle time, from rising edge to rising edge	^{t}DSC (abs)	^{t}DSC(abs) MIN = ^{t}DSC(avg) + ^{t}JITper(DSC) MIN ^{t}DSC(abs) MAX = ^{t}DSC (avg) + ^{t}JITper(DQS) MAX										ns	
Eni LOW until any issued command is ignored	^{t}ENi	–	15	–	15	–	15	–	15	–	15	ns	
CE_# LOW until ENo LOW	^{t}ENo	–	50	–	50	–	50	–	50	–	50	ns	
DQS write preamble	^{t}WPRE	15	–	15	–	15	–	15	–	15	–	ns	
DQS write preamble with ODT enabled	^{t}WPRE2	25	–	25	–	25	–	25	–	25	–	ns	

Table 73: AC Characteristics: NV-DDR2 Command, Address, and Data for modes 0-4

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS write postamble	^{t}WPST	6.5	–	6.5	–	6.5	–	6.5	–	6.5	–	ns	
DQS write postamble hold time	^{t}WPSTH	15	–	15	–	15	–	15	–	15	–	ns	
Data Output													
Access window of DQ[7:0] from CLK	^{t}AC	3	25	3	25	3	25	3	25	3	25	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE and CE# LOW during data burst	^{t}DBS	5	–	5	–	5	–	5	–	5	–	ns	
DQS-DQ skew	^{t}DQSQ	–	2.5	–	2.0	–	1.4	–	1.0	–	0.8	ns	
Access window of DQS from RE# or RE_t / RE_c	^{t}DQSRE	3	25	3	25	3	25	3	25	3	25	ns	
RE# LOW to DQS or DQ[7:0] driven	^{t}DQSD	6	18	6	18	6	18	6	18	6	18	ns	
DQS hold time after RE# LOW or RE_t/ RE_c crosspoint	^{t}DQSRH	5	–	5	–	5	–	5	–	5	–	ns	15
Data valid window	^{t}DVW	^{t}DVW = ^{t}QH - ^{t}DQSQ										ns	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	^{t}QH	0.37	–	0.37	–	0.37	–	0.37	–	0.37	–	^{t}RC (avg)	9, 11
DQS (DQS_t / DQS_c) output HIGH time	^{t}QSH	0.37	–	0.37	–	0.37	–	0.37	–	0.37	–	^{t}RC (avg)	9, 11
DQS (DQS_t / DQS_c) output LOW time	^{t}QSL	0.37	–	0.37	–	0.37	–	0.37	–	0.37	–	^{t}RC (avg)	9, 11
Average RE# cycle time	^{t}RC (avg) or ^{t}RC	30	–	25	–	15	–	12	–	10	–	ns	2
Absolute RE# cycle time	^{t}RC (abs)	^{t}RC(abs) MIN = ^{t}RC(avg) + ^{t}JITper(RE#) MIN ^{t}RC(abs) MAX = $^{\tau}$RC (avg) + ^{t}JITper(RE#) MAX										ns	
Average RE# HIGH hold time	^{t}REH (avg)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	^{t}RC (avg)	4
Absolute RE# HIGH hold time	^{t}REH (abs)	0.43	–	0.43	–	0.43	–	0.43	–	0.43	–	^{t}RC (avg)	
Data output to command, address, or data input	^{t}RHW	100	–	100	–	100	–	100	–	100	–	ns	
Average RE# pulse width	^{t}RP (avg)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	^{t}RC (avg)	4
Average RE# pulse width	^{t}RP (abs)	0.43	–	0.43	–	0.43	–	0.43	–	0.43	–	^{t}RC (avg)	

Table 73: AC Characteristics: NV-DDR2 Command, Address, and Data for modes 0-4

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read preamble with ODT disabled	^{t}RPRE	15	–	15	–	15	–	15	–	15	–	ns	
Read preamble with ODT enabled	^{t}RPRE2	25	–	25	–	25	–	25	–	25	–	ns	
Read postamble	^{t}RPST	^{t}DQSRE + 0.5 * ^{t}RC	–	^{t}DQSRE + 0.5 * ^{t}RC	–	^{t}DQSRE + 0.5 * ^{t}RC	–	^{t}DQSRE + 0.5 * ^{t}RC	–	^{t}DQSRE + 0.5 * ^{t}RC	–	ns	
Read postable hold time	^{t}RPSTH	15	–	15	–	15	–	15	–	15	–	ns	

Notes:
1. ^{t}CHZ and ^{t}CLHZ are not referenced to a specific voltage level, but specify when the device output is no longer driving.
2. The parameters ^{t}RC(avg) and ^{t}DSC(avg) are the average over any 200 consecutive periods and ^{t}RC(avg) / ^{t}DSC(avg) min are the smallest rates allowed, with the exception of a deviation due to ^{t}JIT (per).
3. Input jitter is allowed provided it does not exceed values specified.
4. ^{t}REH(avg) and ^{t}RP(avg) are the average half clock period over any 200 consecutive clocks and is the smallest half period allowed, expect a deviation due to the allowed clock jitter. Input clock jitter is allowed provided it does not exceed values specified.
5. The period jitter ^{t}JIT (per) is the maximum deviation in the ^{t}RC or ^{t}DSC period from the average or nominal ^{t}RC or ^{t}DSC period. It is allowed in either the positive or negative direction.
6. The cycle-to-cycle jitter ^{t}JITcc is the amount the clock period can deviate from one cycle to the next.
7. The duty cycle jitter applies to either the high pulse or low pulse; however, the two cumulatively cannot exceed ^{t}JITper. As long as the absolute minimum half period ^{t}RP(abs), ^{t}REH(abs), ^{t}DQSH or ^{t}DQSL is not less than 43 percent of the average cycle.
8. All timing parameter values assume differential signaling for RE# and DQS is used.
9. When the device is operated with input clock jitter, ^{t}QSL, ^{t}QSH, and ^{t}QH need to be derated by the actual ^{t}JITper in the input clock. (output deratings are relative to the NAND input RE pulse that generated the DQS pulse).
10. The ^{t}DS and ^{t}DH times listed are based on an input slew rate greater than or equal to 1 V/ns for single-ended signal, and based on an input slew rate greater than or equal to 2 V/ns for differential signal. If the input slew rate is less than 1 V/ns for single-ended signal, or less than 2 V/ns for differential signal, then the derating methodology shall be used.
11. When the device is operated with input RE (RE_t/RE_c) jitter, ^{t}QSL, ^{t}QSH, and ^{t}QH need to be derated by the actual input duty cycle jitter beyond 0.45 × ^{t}RC (AVG) but not exceeding 0.43 × ^{t}RC (AVG). Output deratings are relative to the device input RE pulse that generated the DQS pulse.
12. The parameter ^{t}DIPW is defined as the pulse width of the input signal between the first crossing of $V_{REFQ(DC)}$ and the consecutive crossing of $V_{REFQ(DC)}$.
13. ^{t}ADL SPEC for SET FEATURES operations is 70ns.
14. ^{t}CR2 (MIN) is 150ns for read ID sequence only. For all other command sequences ^{t}CR2 (MIN) requirement is 100ns.
15. ^{t}DQSRH is only required if matrix ODT is enabled.
16. Any command (including read status commands) cannot be issued during ^{t}WB, even if R/B# or RDY is ready.
17. ^{t}CS2 shall be applied when the device has any type of ODT enabled including ODT only enabled for data input.

Table 74: AC Characteristics: NV-DDR2 Command, Address, and Data for modes 5-7

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Clock Period		7.5		6		5		ns	
Frequency		≈133		≈166		≈200		MHz	
Command and Address									
Access window of DQ[7:0] from RE# LOW or RE_t/RE_c	^{t}AC	3	25	3	25	3	25	ns	
ALE to data start	^{t}ADL	150	–	150	–	150	–	ns	13
ALE to RE# delay	^{t}AR	10	–	10	–	10	–	ns	
DQ hold–command, address	^{t}CAH	5	–	5	–	5	–	ns	
ALE, CLE hold	^{t}CALH	5	–	5	–	5	–	ns	
ALE, CLE setup with ODT disabled	^{t}CALS	15	–	15	–	15	–	ns	
ALE, CLE setup with ODT enabled	^{t}CALS2	25	–	25	–	25	–	ns	
DQ setup–command, address	^{t}CAS	5	–	5	–	5	–	ns	
CE# HIGH hold time prior to VOLUME SELECT (E1h)	^{t}CEH	20	–	20	–	20	–	ns	
Delay before CE# HIGH for any Volume after a Volume is selected	^{t}CEVDLY	50	–	50	–	50	–	ns	
CE# hold	^{t}CH	5	–	5	–	5	–	ns	
CE# high to output hi-Z	^{t}CHZ	–	30	–	30	–	30	ns	1
CLE high to output hi-Z	^{t}CLHZ	–	30	–	30	–	30	ns	1
CLE to RE# delay	^{t}CLR	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c	^{t}CR	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c if CE# has been HIGH for >1µs	^{t}CR2	100	–	100	–	100	–	ns	
	^{t}CR2 (Read ID)	150	–	150	–	150	–	ns	14
CE# setup time	^{t}CS	20	–	20	–	20	–	ns	
CE# setup for data output with ODT disabled	^{t}CS1	30	–	30	–	30	–	ns	
CE# setup for DQS/DQ[7:0] with ODT enabled	^{t}CS2	40	–	40	–	40	–	ns	17
CE# setup time to DQS (DQS_t) low after CE# has been HIGH for >1µs	^{t}CD	100	–	100	–	100	–	ns	
ALE, CLE, WE#, hold time from CE# HIGH	^{t}CSD	10	–	10	–	10	–	ns	
Eni LOW until any issued command is ignored	^{t}ENi	–	15	–	15	–	15	ns	
CE_# LOW until ENo LOW	^{t}ENo	–	50	–	50	–	50	ns	
Ready to RE# low	^{t}RR	20	–	20	–	20	–	ns	
WE# high to R/B# low	^{t}WB	–	100	–	100	–	100	ns	16
WE# cycle time	^{t}WC	25	–	25	–	25	–	ns	
WE# high hold time	^{t}WH	11	–	11	–	11	–	ns	
WE# high to RE# low	^{t}WHR	80	–	80	–	80	–	ns	

Table 74: AC Characteristics: NV-DDR2 Command, Address, and Data for modes 5-7

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
WE# pulse width	tWP	11	–	11	–	11	–	ns	
WP# transition to WE# low	tWW	100	–	100	–	100	–	ns	
Delay before next command after a Volume is selected	tVDLY	50	–	50	–	50	–	ns	
Jitter									
The deviation of a given tDQS (abs)/tDSC (abs) from a tDQS (avg)/tDCS (avg)	tJITper (DQS)	-0.6	0.6	-0.48	0.48	-0.40	0.40	ns	3, 5, 7
The deviation of a given tRC (abs)/tDSC (abs) from a tRC (avg)/ tDCS (avg)	tJITper (RE#)	-0.45	0.45	-0.36	0.36	-0.30	0.30	ns	3, 5, 7
Cycle to cycle jitter for DQS	tJITcc (DQS)	1.2	–	0.96	–	0.80	–	ns	3, 6
Cycle to cycle jitter for RE#	tJITcc (RE#)	0.9	–	0.72	–	0.60	–	ns	3, 6
Data Input									
DQS setup time for data input	tCDQSS	30	–	30	–	30	–	ns	
DQS hold time for data input burst end	tCDQSH	100	–	100	–	100	–	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE and CE# LOW during data burst	tDBS	5	–	5	–	5	–	ns	
Data hold time	tDH	0.6	–	0.55	–	0.40	–	ns	10
Data setup time	tDS	0.6	–	0.55	–	0.40	–	ns	10
DQ input pulse width	tDIPW	0.31	–	0.31	–	0.31	–	tDSC (avg)	12
DQS input high pulse width	tDQSH	0.43	–	0.43	–	0.43	–	tDSC (avg)	
DQS input low pulse width	tDQSL	0.43	–	0.43	–	0.43	–	tDSC (avg)	
Average DQS cycle time	tDSC (avg) or tDSC	7.5	–	6	–	5	–	ns	2
Absolute DQS cycle time, from rising edge to rising edge	tDSC (abs)	tDSC(abs) MIN = tDSC(avg) + tJITper(DSC) MIN tDSC(abs) MAX = τDSC (avg) + tJITper(DQS) MAX						ns	
Eni LOW until any issued command is ignored	tENi	–	15	–	15	–	15	ns	
CE_# LOW until ENo LOW	tENo	–	50	–	50	–	50	ns	
DQS write preamble	tWPRE	15	–	15	–	15	–	ns	
DQS write preamble with ODT enabled	tWPRE2	25	–	25	–	25	–	ns	
DQS write postamble	tWPST	6.5	–	6.5	–	6.5	–	ns	
DQS write postamble hold time	tWPSTH	15	–	15	–	15	–	ns	
Data Output									
Access window of DQ[7:0] from CLK	tAC	3	25	3	25	3	25	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE and CE# LOW during data burst	tDBS	5	–	5	–	5	–	ns	

Table 74: AC Characteristics: NV-DDR2 Command, Address, and Data for modes 5-7

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
DQS-DQ skew	^{t}DQSQ	–	0.6	–	0.5	–	0.4	ns	
Access window of DQS from RE# or RE_t / RE_c	^{t}DQSRE	3	25	3	25	3	25	ns	
RE# LOW to DQS or DQ[7:0] driven	^{t}DQSD	6	18	6	18	6	18	ns	
DQS hold time after RE# LOW or RE_t/RE_c crosspoint	^{t}DQSRH	5	–	5	–	5	–	ns	15
Data valid window	^{t}DVW	^{t}DVW = ^{t}QH - ^{t}DQSQ						ns	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	^{t}QH	0.37	–	0.37	–	0.37	–	^{t}RC (avg)	9, 11
DQS (DQS_t / DQS_c) output HIGH time	^{t}QSH	0.37	–	0.37	–	0.37	–	^{t}RC (avg)	9, 11
DQS (DQS_t / DQS_c) output LOW time	^{t}QSL	0.37	–	0.37	–	0.37	–	^{t}RC (avg)	9, 11
Average RE# cycle time	^{t}RC (avg) or ^{t}RC	7.5	–	6	–	5	–	ns	2
Absolute RE# cycle time	^{t}RC (abs)	^{t}RC(abs) MIN = ^{t}RC(avg) + ^{t}JITper(RE#) MIN ^{t}RC(abs) MAX = ^{t}RC (avg) + ^{t}JITper(RE#) MAX						ns	
Average RE# HIGH hold time	^{t}REH (avg)	0.45	0.55	0.45	0.55	0.45	0.55	^{t}RC (avg)	4
Absolute RE# HIGH hold time	^{t}REH (abs)	0.43	–	0.43	–	0.43	–	^{t}RC (avg)	
Data output to command, address, or data input	^{t}RHW	100	–	100	–	100	–	ns	
Average RE# pulse width	^{t}RP (avg)	0.45	0.55	0.45	0.55	0.45	0.55	^{t}RC (avg)	4
Average RE# pulse width	^{t}RP (abs)	0.43	–	0.43	–	0.43	–	^{t}RC (avg)	
Read preamble with ODT disabled	^{t}RPRE	15	–	15	–	15	–	ns	
Read preamble with ODT enabled	^{t}RPRE2	25	–	25	–	25	–	ns	
Read postamble	^{t}RPST	^{t}DQSRE + 0.5 * ^{t}RC	–	^{t}DQSRE + 0.5 * ^{t}RC	–	^{t}DQSRE + 0.5 * ^{t}RC	–	ns	
Read postable hold time	^{t}RPSTH	15	–	15	–	15	–	ns	

Notes:
1. ^{t}CHZ and ^{t}CLHZ are not referenced to a specific voltage level, but specify when the device output is no longer driving.
2. The parameters ^{t}RC(avg) and ^{t}DSC(avg) are the average over any 200 consecutive periods and ^{t}RC(avg) / ^{t}DSC(avg) min are the smallest rates allowed, with the exception of a deviation due to ^{t}JIT (per).
3. Input jitter is allowed provided it does not exceed values specified.
4. ^{t}REH(avg) and ^{t}RP(avg) are the average half clock period over any 200 consecutive clocks and is the smallest half period allowed, expect a deviation due to the allowed clock jitter. Input clock jitter is allowed provided it does not exceed values specified.

5. The period jitter ^{t}JIT (per) is the maximum deviation in the ^{t}RC or ^{t}DSC period from the average or nominal ^{t}RC or ^{t}DSC period. It is allowed in either the positive or negative direction.
6. The cycle-to-cycle jitter ^{t}JITcc is the amount the clock period can deviate from one cycle to the next.
7. The duty cycle jitter applies to either the high pulse or low pulse; however, the two cumulatively cannot exceed ^{t}JITper. As long as the absolute minimum half period ^{t}RP(abs), ^{t}REH(abs), ^{t}DQSH or ^{t}DQSL is not less than 43 percent of the average cycle.
8. All timing parameter values assume differential signaling for RE# and DQS is used.
9. When the device is operated with input clock jitter, ^{t}QSL, ^{t}QSH, and ^{t}QH need to be derated by the actual ^{t}JITper in the input clock. (output deratings are relative to the NAND input RE pulse that generated the DQS pulse).
10. The ^{t}DS and ^{t}DH times listed are based on an input slew rate of 1 V/ns. If the input slew rate is not 1 V/ns, then the derating methodology shall be used.
11. When the device is operated with input RE (RE_t/RE_c) jitter, ^{t}QSL, ^{t}QSH, and ^{t}QH need to be derated by the actual input duty cycle jitter beyond 0.45 × ^{t}RC (AVG) but not exceeding 0.43 × ^{t}RC (AVG). Output deratings are relative to the device input RE pulse that generated the DQS pulse.
12. The parameter ^{t}DIPW is defined as the pulse width of the input signal between the first crossing of $V_{REFQ(DC)}$ and the consecutive crossing of $V_{REFQ(DC)}$.
13. ^{t}ADL SPEC for SET FEATURES operations is 70ns.
14. ^{t}CR2 (MIN) is 150ns for Read ID sequence only. For all other command sequences ^{t}CR2 (MIN) requirement is 100ns.
15. ^{t}DQSRH is only required if matrix ODT is enabled.
16. Any command (including read status commands) cannot be issued during ^{t}WB, even if R/B# or RDY is ready.
17. ^{t}CS2 shall be applied when the device has any type of ODT enabled including ODT only enabled for data input.

Table 75: AC Characteristics: NV-DDR2 Command, Address, and Data for modes 8-9

Parameter	Symbol	Mode 8		Mode 9		Unit	Notes
		Min	Max	Min	Max		
Clock Period		3.75		3		ns	
Frequency		≈266		≈333		MHz	
Command and Address							
Access window of DQ[7:0] from RE# LOW or RE_t/RE_c	^{t}AC	3	25	3	25	ns	
ALE to data start	^{t}ADL	150	–	150	–	ns	1
ALE to RE# delay	^{t}AR	10	–	10	–	ns	
DQ hold–command, address	^{t}CAH	5	–	5	–	ns	
ALE, CLE hold	^{t}CALH	5	–	5	–	ns	
ALE, CLE setup with ODT disabled	^{t}CALS	15	–	15	–	ns	
ALE, CLE setup with ODT enabled	^{t}CALS2	25	–	25	–	ns	
DQ setup–command, address	^{t}CAS	5	–	5	–	ns	
CE# HIGH hold time prior to VOLUME SELECT (E1h)	^{t}CEH	20	–	20	–	ns	
Delay before CE# HIGH for any Volume after a Volume is selected	^{t}CEVDLY	50	–	50	–	ns	
CE# hold	^{t}CH	5	–	5	–	ns	
CE# high to output hi-Z	^{t}CHZ	–	30	–	30	ns	2

Table 75: AC Characteristics: NV-DDR2 Command, Address, and Data for modes 8-9

Parameter	Symbol	Mode 8		Mode 9		Unit	Notes
		Min	Max	Min	Max		
CLE high to output hi-Z	tCLHZ	–	30	–	30	ns	2
CLE to RE# delay	tCLR	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c	tCR	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c if CE# has been HIGH for >1µs	tCR2	100	–	100	–	ns	
	tCR2 (Read ID)	150	–	150	–	ns	15
CE# setup time	tCS	20	–	20	–	ns	
CE# setup for data output with ODT disabled	tCS1	30	–	30	–	ns	
CE# setup for DQS/DQ[7:0] with ODT enabled	tCS2	40	–	40	–	ns	19
CE# setup time to DQS (DQS_t) low after CE# has been HIGH for >1µs	tCD	100	–	100	–	ns	
ALE, CLE, WE#, hold time from CE# HIGH	tCSD	10	–	10	–	ns	
Eni LOW until any issued command is ignored	tENi	–	15	–	15	ns	
CE_# LOW until ENo LOW	tENo	–	50	–	50	ns	
Ready to RE# low	tRR	20	–	20	–	ns	
WE# high to R/B# low	tWB	–	100	–	100	ns	18
WE# cycle time	tWC	25	–	25	–	ns	
WE# high hold time	tWH	11	–	11	–	ns	
WE# high to RE# low	tWHR	80	–	80	–	ns	
WE# pulse width	tWP	11	–	11	–	ns	
WP# transition to WE# low	tWW	100	–	100	–	ns	
Delay before next command after a Volume is selected	tVDLY	50	–	50	–	ns	
Jitter							
The deviation of a given tDQS (abs)/tDSC (abs) from a tDQS (avg)/tDCS (avg)	tJITper (DQS)	-0.30	0.30	-0.24	0.24	ns	4, 6, 8
The deviation of a given tRC (abs)/tDSC (abs) from a tRC (avg)/tDCS (avg)	tJITper (RE#)	-0.225	0.225	-0.18	0.18	ns	4, 6, 8
Cycle to cycle jitter for DQS	tJITcc (DQS)	0.6	–	0.48	–	ns	4, 7
Cycle to cycle jitter for RE#	tJITcc (RE#)	0.45	–	0.36	–	ns	4, 7
Data Input							
DQS setup time for data input	tCDQSS	30	–	30	–	ns	
DQS hold time for data input burst end	tCDQSH	100	–	100	–	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE and CE# LOW during data burst	tDBS	5	–	5	–	ns	
Data hold time	tDH	0.30	–	0.24	–	ns	11
Data setup time	tDS	0.30	–	0.24	–	ns	11
DQ input pulse width	tDIPW	0.31	–	0.31	–	tDSC (avg)	13

Table 75: AC Characteristics: NV-DDR2 Command, Address, and Data for modes 8-9

Parameter	Symbol	Mode 8		Mode 9		Unit	Notes
		Min	Max	Min	Max		
DQS input high pulse width	^{t}DQSH	0.43	–	0.43	–	^{t}DSC (avg)	
DQS input low pulse width	^{t}DQSL	0.43	–	0.43	–	^{t}DSC (avg)	
Average DQS cycle time	^{t}DSC (avg) or ^{t}DSC	3.75	–	3	–	ns	3
Absolute DQS cycle time, from rising edge to rising edge	^{t}DSC (abs)	^{t}DSC (ABS) MIN = ^{t}DSC (AVG) + ^{t}JITper(DQS) MIN ^{t}DSC (ABS) MAX = ^{t}DSC (AVG) + ^{t}JITper(DQS) MAX				ns	
Eni LOW until any issued command is ignored	^{t}ENi	–	15	–	15	ns	
CE_# LOW until ENo LOW	^{t}ENo	–	50	–	50	ns	
DQS write preamble	^{t}WPRE	15	–	15	–	ns	
DQS write preamble with ODT enabled	^{t}WPRE2	25	–	25	–	ns	
DQS write postamble	^{t}WPST	6.5	–	6.5	–	ns	
DQS write postamble hold time	^{t}WPSTH	15	–	15	–	ns	
Data Output							
Access window of DQ[7:0] from CLK	^{t}AC	3	25	3	25	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE and CE# LOW during data burst	^{t}DBS	5	–	5	–	ns	
DQS-DQ skew	^{t}DQSQ	–	0.350	–	0.30	ns	
Access window of DQS from RE# or RE_t / RE_c	^{t}DQSRE	3	25	3	25	ns	
RE# LOW to DQS or DQ[7:0] driven	^{t}DQSD	6	18	6	18	ns	
DQS hold time after RE# LOW or RE_t/ RE_c crosspoint	^{t}DQSRH	5	–	5	–	ns	16
Data valid window	^{t}DVW	^{t}DVW = ^{t}QH - ^{t}DQSQ				ns	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	^{t}QH	0.37	–	0.37	–	^{t}RC (avg)	10, 12
DQS (DQS_t / DQS_c) output HIGH time	^{t}QSH	0.37	–	0.37	–	^{t}RC (avg)	10, 12
DQS (DQS_t / DQS_c) output LOW time	^{t}QSL	0.37	–	0.37	–	^{t}RC (avg)	10, 12
Average RE# cycle time	^{t}RC (avg) or ^{t}RC	3.75	–	3	–	ns	3
Absolute RE# cycle time	^{t}RC (abs)	^{t}RC (ABS) MIN = ^{t}RC (AVG) + ^{t}JITper(RE#) MIN ^{t}RC (ABS) MAX = ^{t}RC (AVG) + ^{t}JITper(RE#) MAX				ns	
Average RE# HIGH hold time	^{t}REH (avg)	0.45	0.55	0.45	0.55	^{t}RC (avg)	5
Absolute RE# HIGH hold time	^{t}REH (abs)	0.43	–	0.43	–	^{t}RC (avg)	
Data output to command, address, or data input	^{t}RHW	100	–	100	–	ns	

Table 75: AC Characteristics: NV-DDR2 Command, Address, and Data for modes 8-9

Parameter	Symbol	Mode 8		Mode 9		Unit	Notes
		Min	Max	Min	Max		
Average RE# pulse width	^{t}RP (avg)	0.45	0.55	0.45	0.55	^{t}RC (avg)	5
Average RE# pulse width	^{t}RP (abs)	0.43	–	0.43	–	^{t}RC (avg)	
Read preamble with ODT disabled	^{t}RPRE	15	–	15	–	ns	
Read preamble with ODT enabled	^{t}RPRE2	25	–	25	–	ns	
Read postamble	^{t}RPST	^{t}DQS RE + 0.5 * ^{t}RC	–	^{t}DQS RE + 0.5 * ^{t}RC	–	ns	
Read postable hold time	^{t}RPSTH	15	–	15	–	ns	

Notes:
1. ^{t}ADL for SET FEATURES operations is 100ns.
2. ^{t}CHZ and ^{t}CLHZ are not referenced to a specific voltage level, but specify when the device output is no longer driving.
3. The parameters ^{t}RC (AVG) and ^{t}DSC (AVG) are the average over any 200 consecutive periods and ^{t}RC (AVG)/^{t}DSC (AVG) min are the smallest rates allowed, with the exception of a deviation due to ^{t}JIT (per).
4. Input jitter is allowed provided it does not exceed values specified.
5. ^{t}REH (AVG) and ^{t}RP (AVG) are the average half clock period over any 200 consecutive clocks and is the smallest half period allowed, expect a deviation due to the allowed clock jitter. Input clock jitter is allowed provided it does not exceed values specified.
6. The period jitter ^{t}JIT (per) is the maximum deviation in the ^{t}RC or ^{t}DSC period from the average or nominal ^{t}RC or ^{t}DSC period. It is allowed in either the positive or negative direction.
7. The cycle-to-cycle jitter ^{t}JITcc is the amount the clock period can deviate from one cycle to the next.
8. The duty cycle jitter applies to either the high pulse or low pulse; however, the two cumulatively cannot exceed ^{t}JITper. As long as the absolute minimum half period ^{t}RP (ABS), ^{t}REH (ABS), ^{t}DQSH, or ^{t}DQSL is not less than 43 percent of the average cycle.
9. All timing parameter values assume differential signaling for RE# and DQS is used.
10. When the device is operated with input clock jitter, ^{t}QSL, ^{t}QSH, and ^{t}QH need to be derated by the actual ^{t}JITper in the input clock. (output deratings are relative to the NAND input RE pulse that generated the DQS pulse).
11. The ^{t}DS and ^{t}DH times listed are based on an input slew rate greater than or equal to 1 V/ns for single-ended signal, and based on an input slew rate greater than or equal to 2 V/ns for differential signal. If the input slew rate is less than 1 V/ns for single-ended signal, or less than 2 V/ns for differential signal, then the derating methodology shall be used.
12. When the device is operated with input RE (RE_t/RE_c) jitter, ^{t}QSL, ^{t}QSH, and ^{t}QH need to be derated by the actual input duty cycle jitter beyond 0.45 × ^{t}RC (AVG) but not exceeding 0.43 × ^{t}RC (AVG). Output deratings are relative to the device input RE pulse that generated the DQS pulse.
13. The parameter ^{t}DIPW is defined as the pulse width of the input signal between the first crossing of $V_{REFQ(DC)}$ and the consecutive crossing of $V_{REFQ(DC)}$.
14. ^{t}ADL SPEC for SET FEATURES operations is 70ns.
15. ^{t}CR2 (MIN) is 150ns for Read ID sequence only. For all other command sequences ^{t}CR2 (MIN) requirement is 100ns.
16. ^{t}DQSRH is only required if matrix ODT is enabled.

17. Parameters ^{t}DQSQ and ^{t}QH are used to calculate overall ^{t}DVW (^{t}DVW = ^{t}QH - ^{t}DQSQ). Since data eye training to optimize strobe placement is expected at high I/O speeds (≥533 MT/s), ^{t}DQSQ and ^{t}QH may borrow time from each other without changing ^{t}DVW. For example, if there exists X ps of margin on ^{t}DQSQ, then ^{t}QH can be provided with an additional X ps without changing the value of ^{t}DVW. When timing margin is borrowed from ^{t}DQSQ to provide additional timing for ^{t}QH, the same amount of timing margin can be used for additional timing for ^{t}QSL or ^{t}QSH.
18. Any command (including read status commands) cannot be issued during ^{t}WB, even if R/B# or RDY is ready.
19. ^{t}CS2 shall be applied when the device has any type of ODT enabled including ODT only enabled for data input.

Electrical Specification – Array Characteristics

Table 76: Array Characteristics

Parameter	Symbol	Max	Unit	Notes
Number of partial page programs	NOP	1	Cycles	1
ERASE BLOCK operation time	^{t}BERS	30	ms	7
Cache busy	^{t}CBSY	2060	µs	6
Change column setup time to data in/out or next command	^{t}CCS	400	ns	
Dummy busy time	^{t}DBSY	1	µs	
ERASE SUSPEND operation time	^{t}ESPD	300	µs	
Busy time when ERASE SUSPEND is issued when LUN is already in the suspend state or ERASE RESUME is issued when no erase is suspended or ongoing	^{t}ESPDN	18	µs	
Busy time for SET FEATURES and GET FEATURES operations	^{t}FEAT	1	µs	
Busy time for interface change	^{t}ITC	1	µs	2
LAST PAGE PROGRAM operation time	^{t}LPROG	–	µs	3
Power-on reset time	^{t}POR	3	ms	
PROGRAM PAGE operation time (single-pass programming - per page)	^{t}PROG_eff	1030	µs	
PROGRAM PAGE operation time	^{t}PROG	2060	µs	6
Page buffer transfer busy time	^{t}PBSY	34	µs	
PROGRAM SUSPEND operation time	^{t}PBPD	150	µs	
PROGRAM SUSPEND operation time during cache programming		2060	µs	
Busy time when PROGRAM SUSPEND is issued when LUN is already in suspend state or PROGRAM RESUME is issued when no program is suspended or ongoing	^{t}PSPDN	18	µs	
Internal randomization time	^{t}RAND	25	µs	8
MULTI PLANE READ PAGE operation time	^{t}R	73	µs	5
SINGLE PLANE READ PAGE operation time	^{t}R_SP	71	µs	5
Cache read busy time	^{t}RCBSY	73	µs	5
MULTI-PLANE EXPRESS READ operation time	^{t}RER	71	µs	8
SINGLE PLANE EXPRESS READ operation time	^{t}RER_SP	69	µs	8
SNAP READ operation time	^{t}RSNAP	51	µs	8
Device reset time (Read/Program/Erase)	^{t}RST	10/30/500	µs	4
Busy time for GET FEATURES operation for temperature sensor readout	^{t}TEMP	120	µs	

Notes:
1. The pages in the OTP Block have an NOP of 2.
2. ^{t}ITC (MAX) is the busy time when the interface changes from Asynchronous to NV-DDR/NV-DDR2 using the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command or NV-DDR/NV-DDR2 to asynchronous using the RESET (FFh) command. During the ^{t}ITC time, any command, including READ STATUS (70h) and READ STATUS ENHANCED (78h), is prohibited.
3. ^{t}LPROG = ^{t}PROG (last page) + ^{t}PROG (last page - 1) - command load time (last page) - address load time (last page) - data load time (last page).
4. If RESET command is issued when the target is READY, the target goes busy for a maximum of 5µs.
5. For read retry options 8 to 15, ^{t}R and ^{t}RCBSY (MAX) may be up to TBD µs.
6. In the case of a program operation that exceeds ^{t}PROG/^{t}CBSY Max, that specific NAND block may be retired by the host system.
7. In the case of an erase operation that exceeds ^{t}BERS Max, that specific NAND block may be retired by the host system.
8. With randomizer enabled, the total array read time for a given parameter will be the value of that parameter + ^{t}RAND.

Table 77: SLC Array Characteristics

Parameter	Symbol	Max	Unit	Notes
Number of partial page programs	NOP	1	Cycles	
ERASE BLOCK operation time	^{t}BERS	30	ms	4
Cache busy	^{t}CBSY	2060	µs	3
LAST PAGE PROGRAM operation time	^{t}LPROG	–	µs	1
PROGRAM PAGE operation time	^{t}PROG	2060	µs	3
MULTI PLANE READ PAGE operation time	^{t}R	73	µs	2
SINGLE PLANE READ PAGE operation time	^{t}R_SP	71	µs	2
Cache read busy time	^{t}RCBSY	73	µs	2
MULTI-PLANE EXPRESS READ operation time	^{t}RER	71	µs	5
SINGLE PLANE EXPRESS READ operation time	^{t}RER_SP	69	µs	5
SNAP READ operation time	^{t}RSNAP	51	µs	5

Notes:
1. ^{t}LPROG = ^{t}PROG (last page) + ^{t}PROG (last page - 1) - command load time (last page) - address load time (last page) - data load time (last page).
2. For read retry options 8 to 15, ^{t}R and ^{t}RCBSY (MAX) may be up to 180µs.
3. In the case of a PROGRAM operation that exceeds ^{t}PROG/tCBSY (MAX), that specific NAND block may be retired by the host system.
4. In the case of a ERASE operation that exceeds ^{t}BERS (MAX), that specific NAND block may be retired by the host system.
5. With randomizer enabled, the total array read time for a given parameter will be the value of that parameter + ^{t}RAND.

Asynchronous Interface Timing Diagrams

Figure 91: RESET Operation

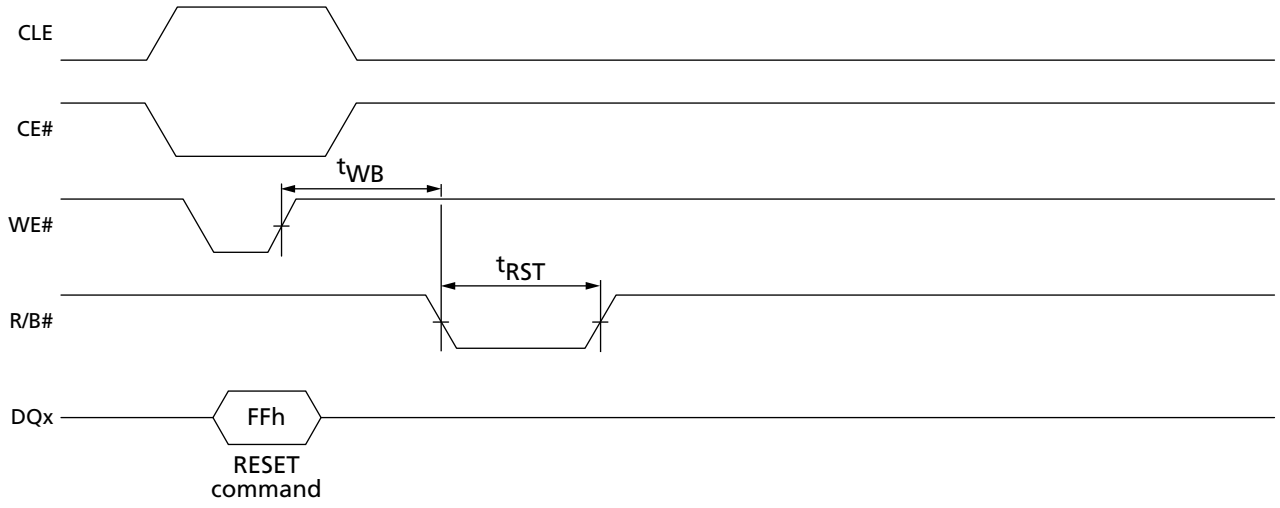


Figure 92: RESET by LUN Operation

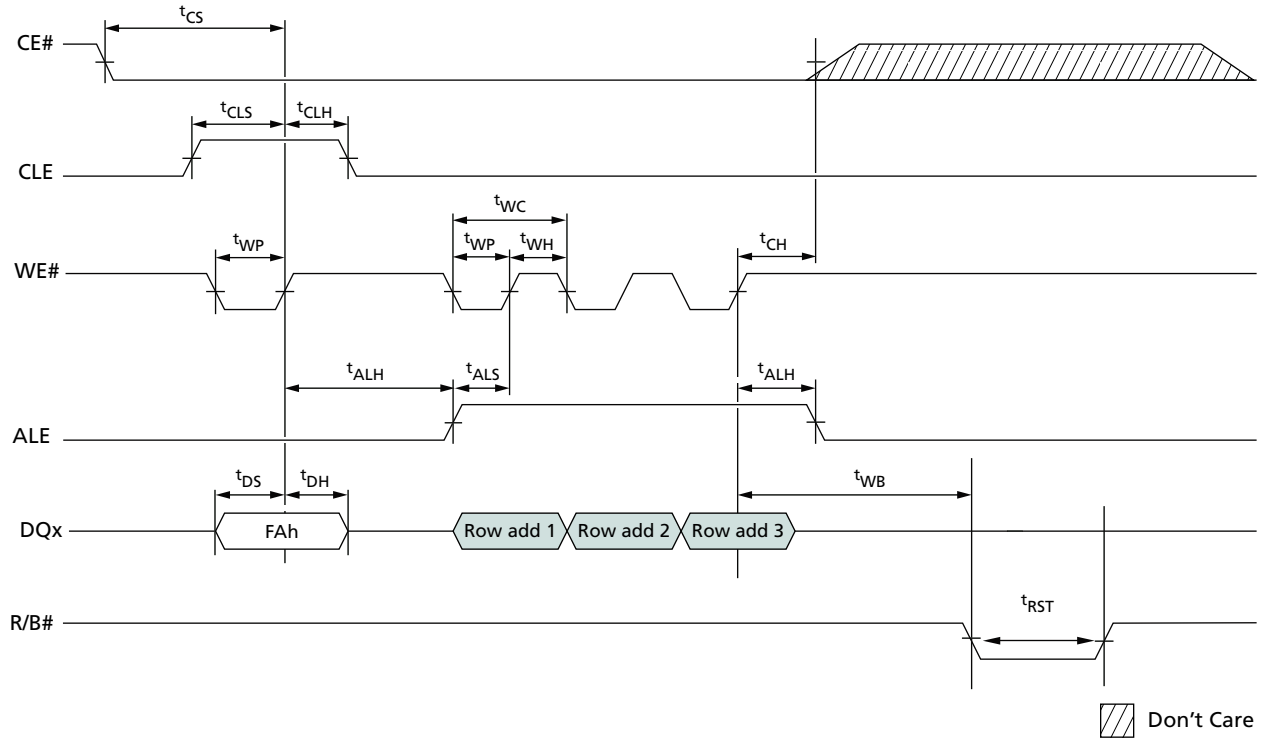


Figure 93: READ STATUS Cycle

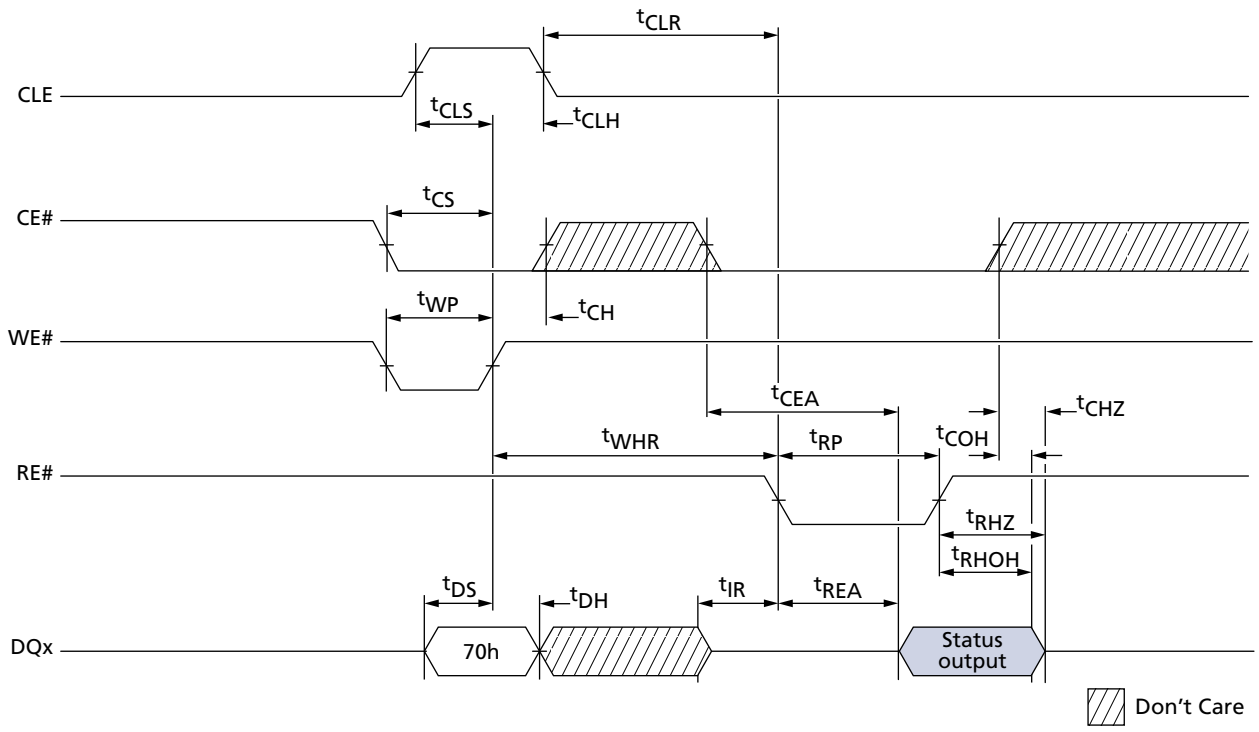


Figure 94: READ STATUS ENHANCED Cycle

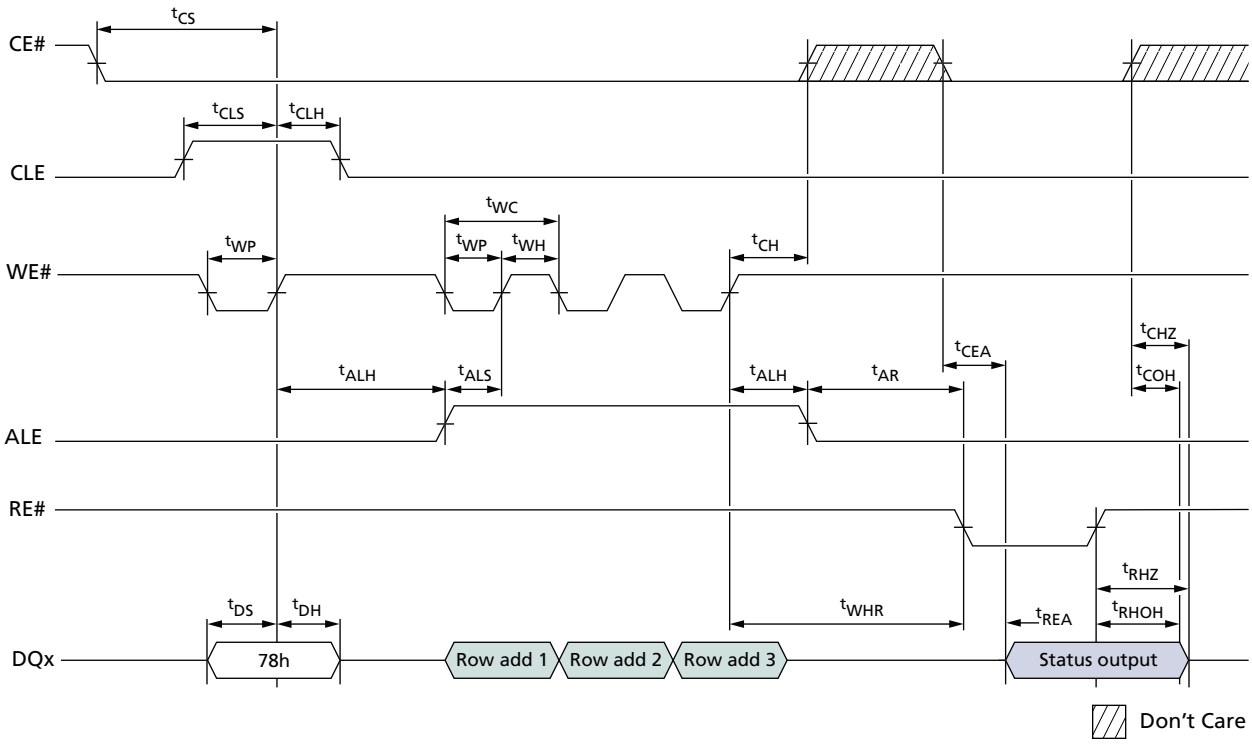


Figure 95: READ PARAMETER PAGE

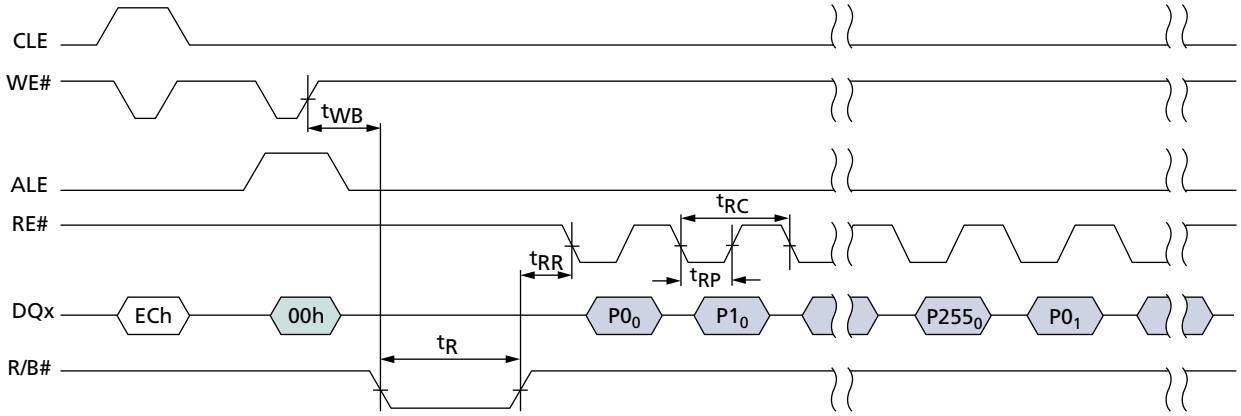


Figure 96: READ PAGE

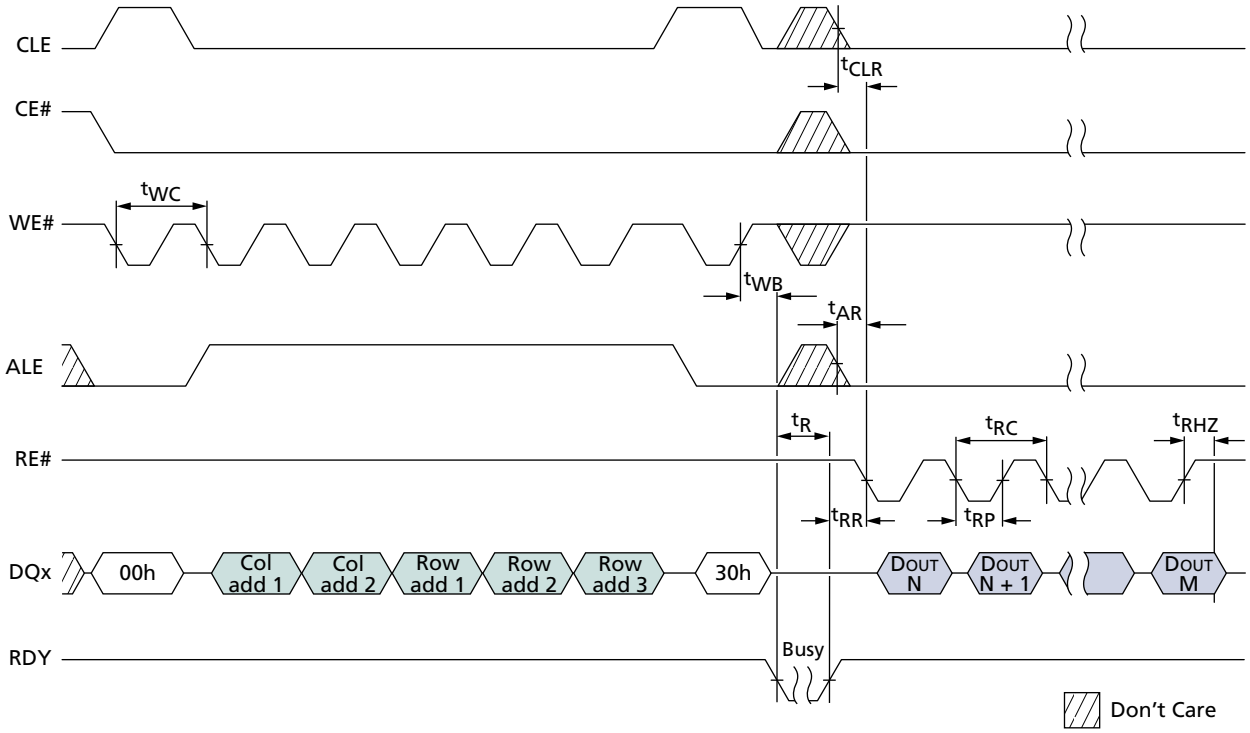


Figure 97: READ PAGE Operation with CE# "Don't Care"

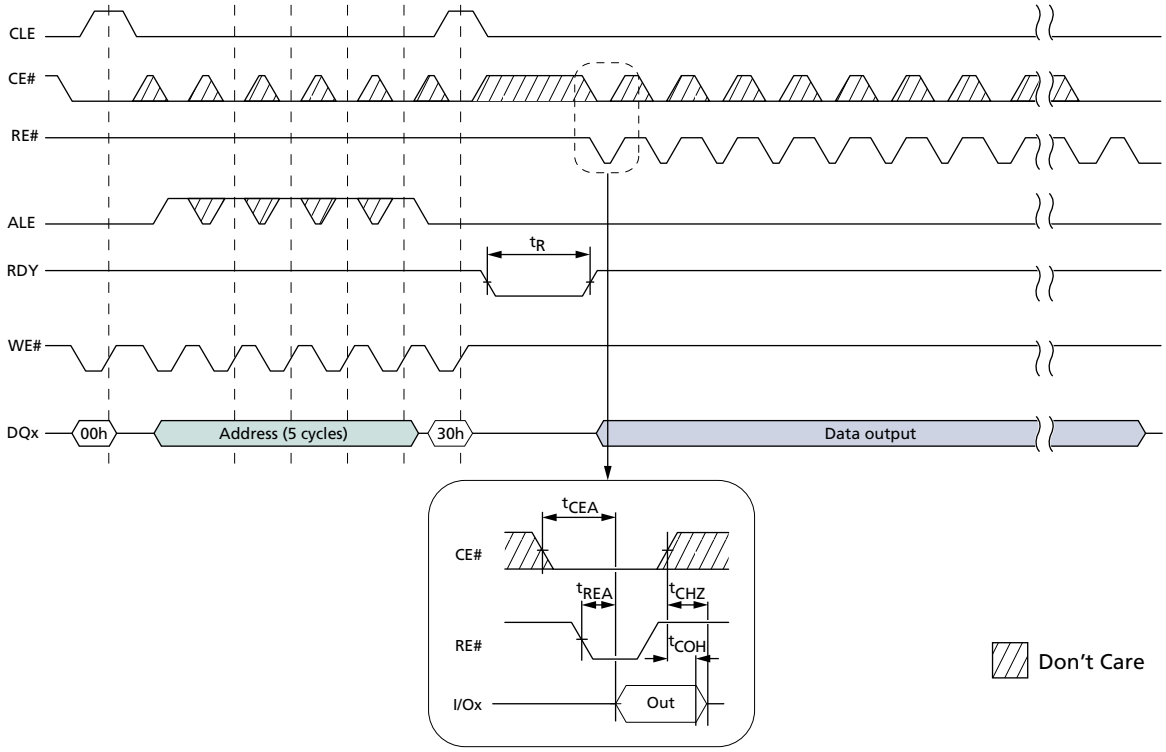


Figure 98: CHANGE READ COLUMN

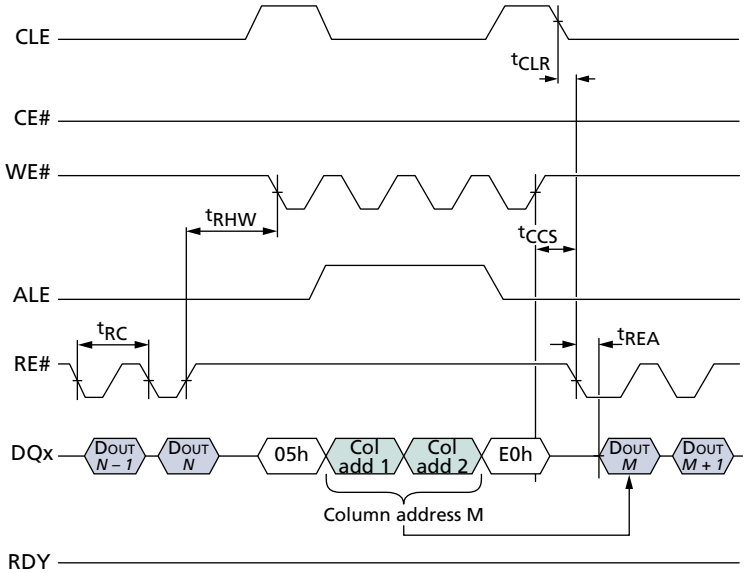


Figure 99: READ ID Operation

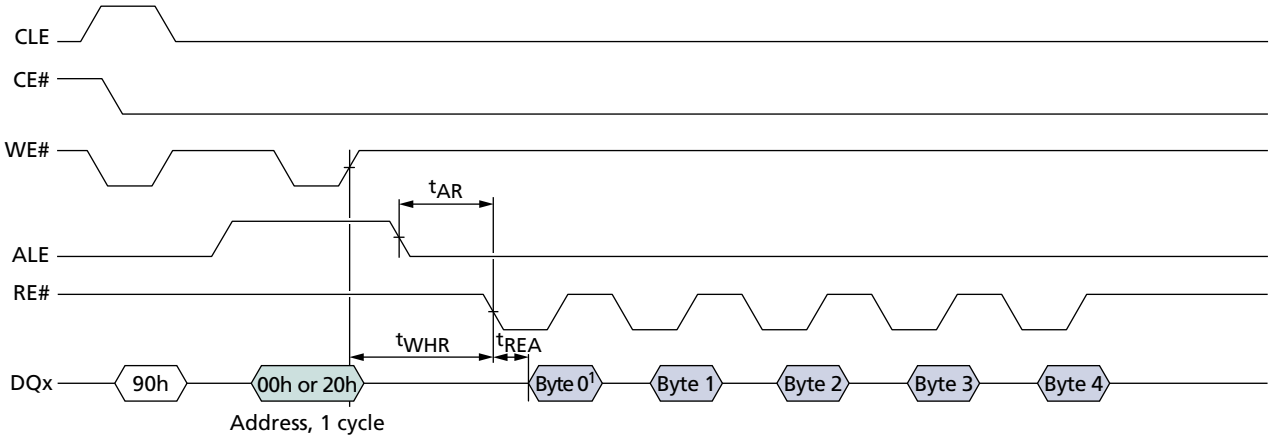


Figure 100: PROGRAM PAGE Operation

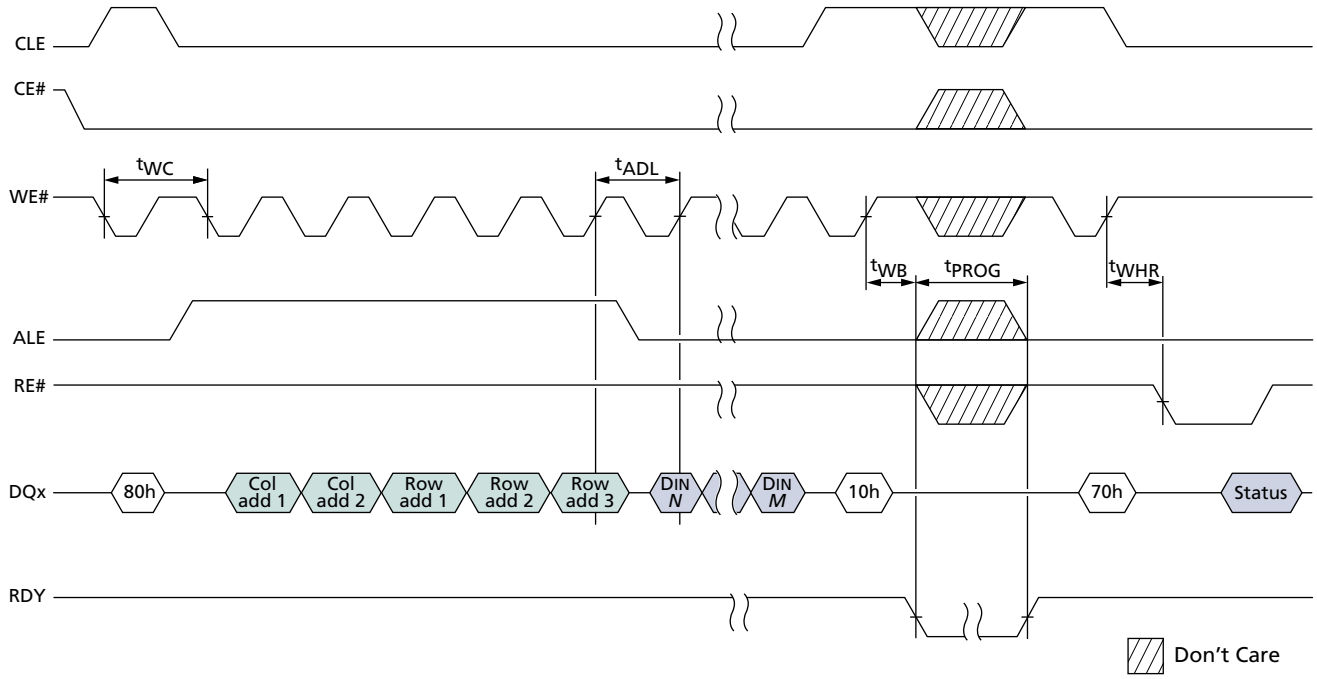


Figure 101: PROGRAM PAGE Operation with CE# "Don't Care"

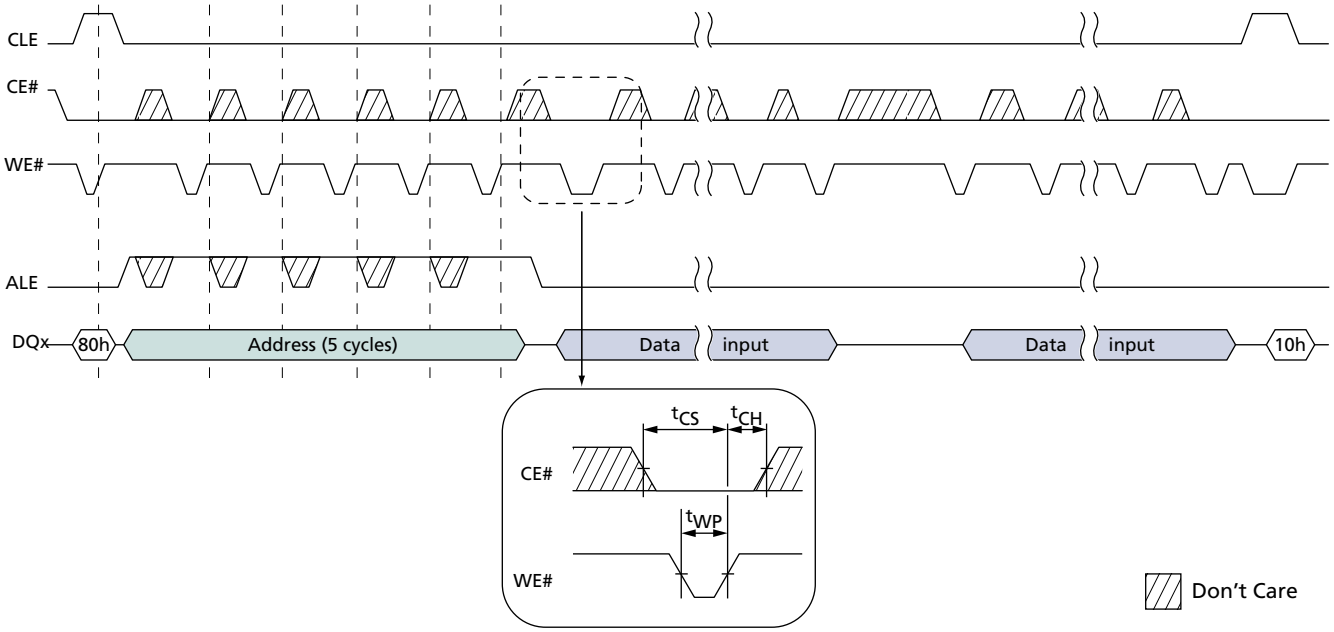


Figure 102: PROGRAM PAGE Operation with CHANGE WRITE COLUMN

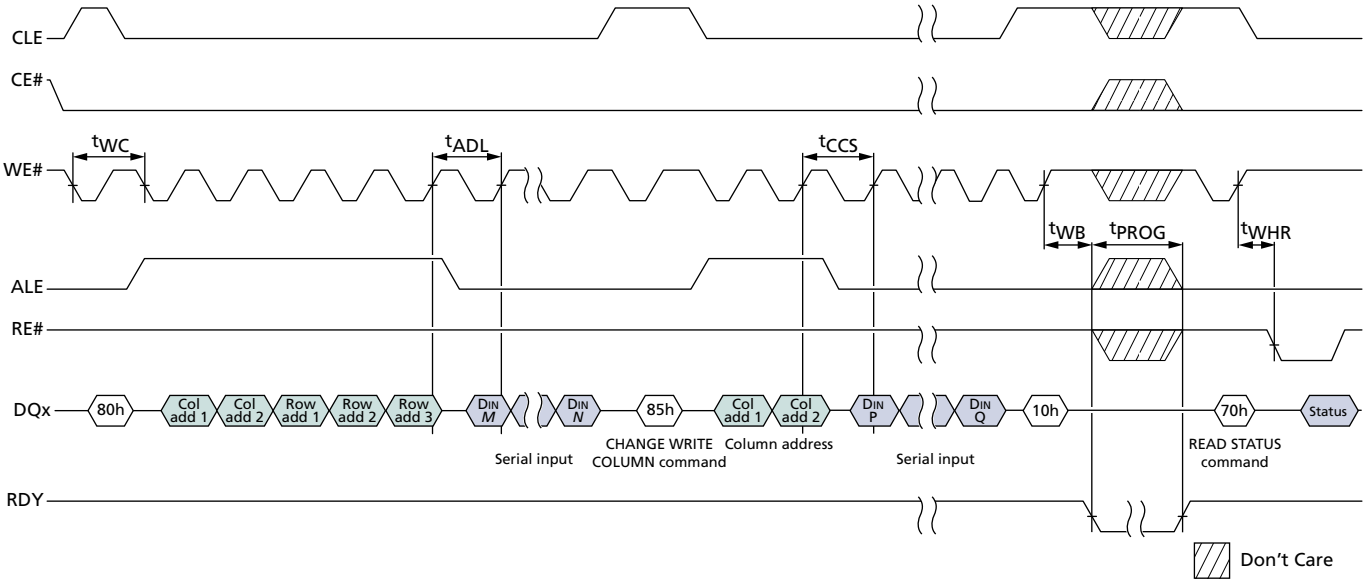


Figure 103: PROGRAM PAGE CACHE

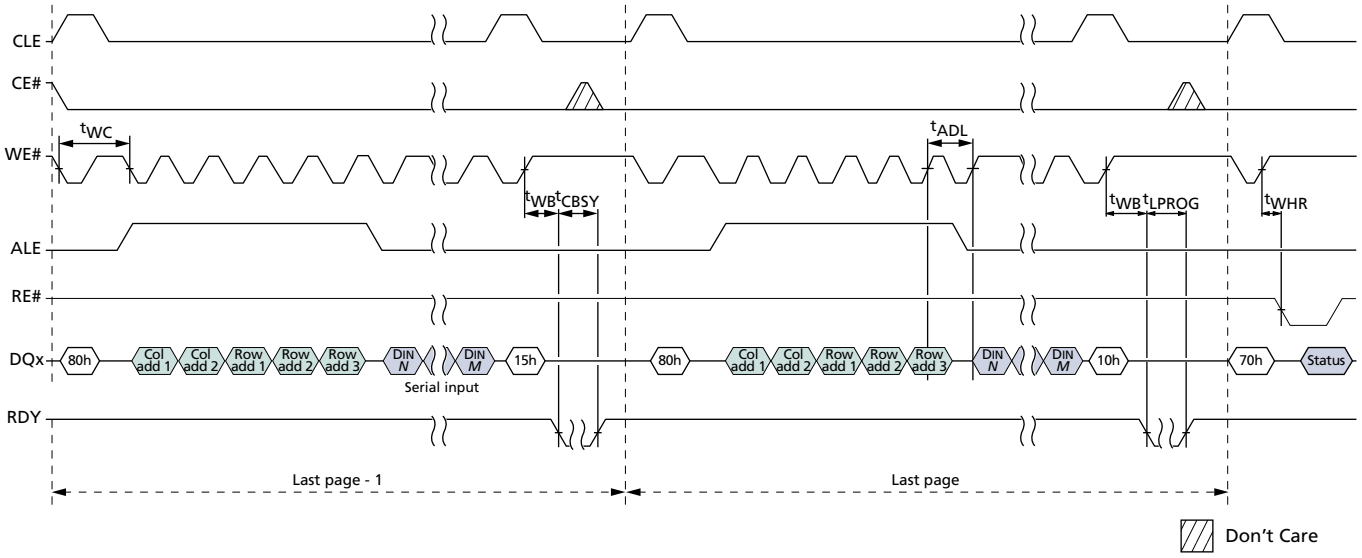


Figure 104: PROGRAM PAGE CACHE Ending on 15h

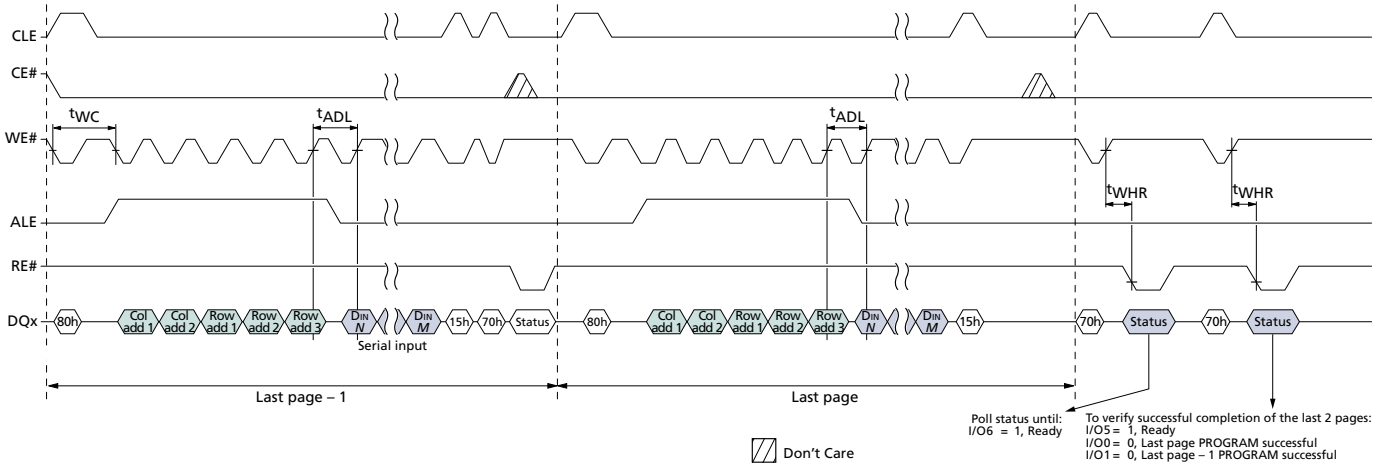


Figure 105: COPYBACK

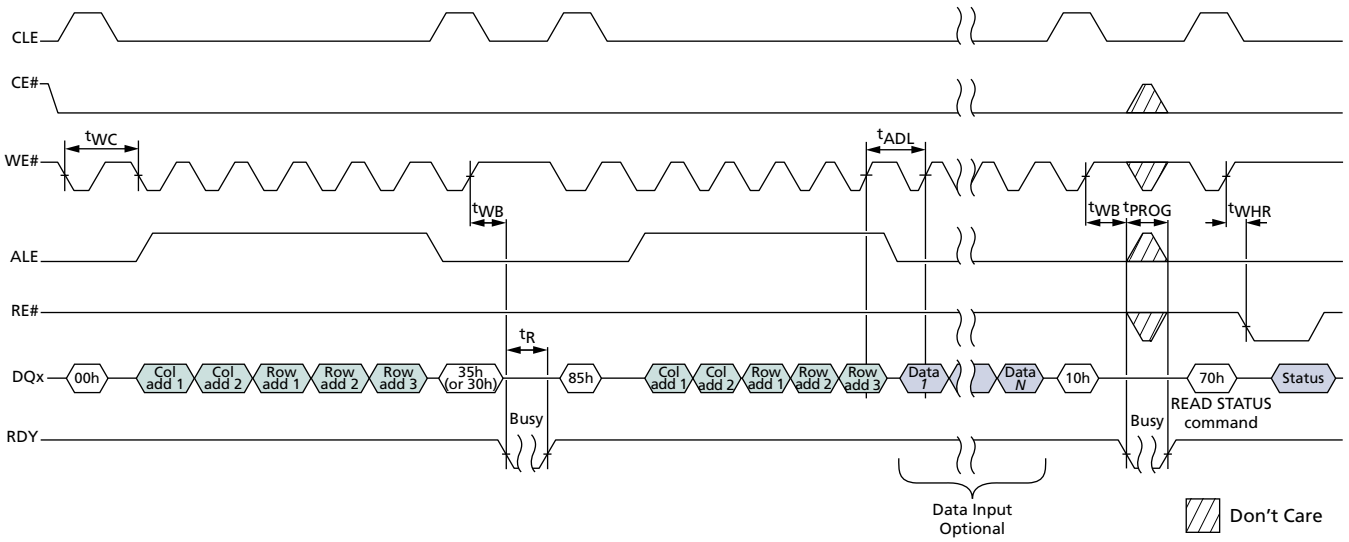
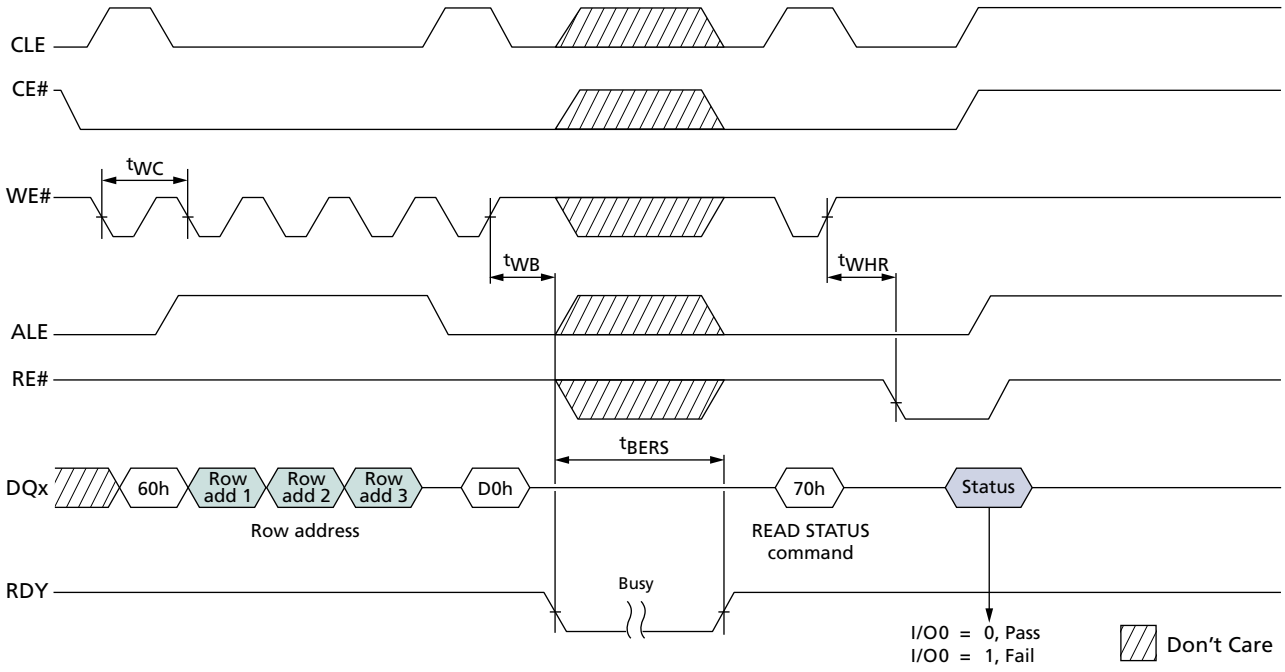
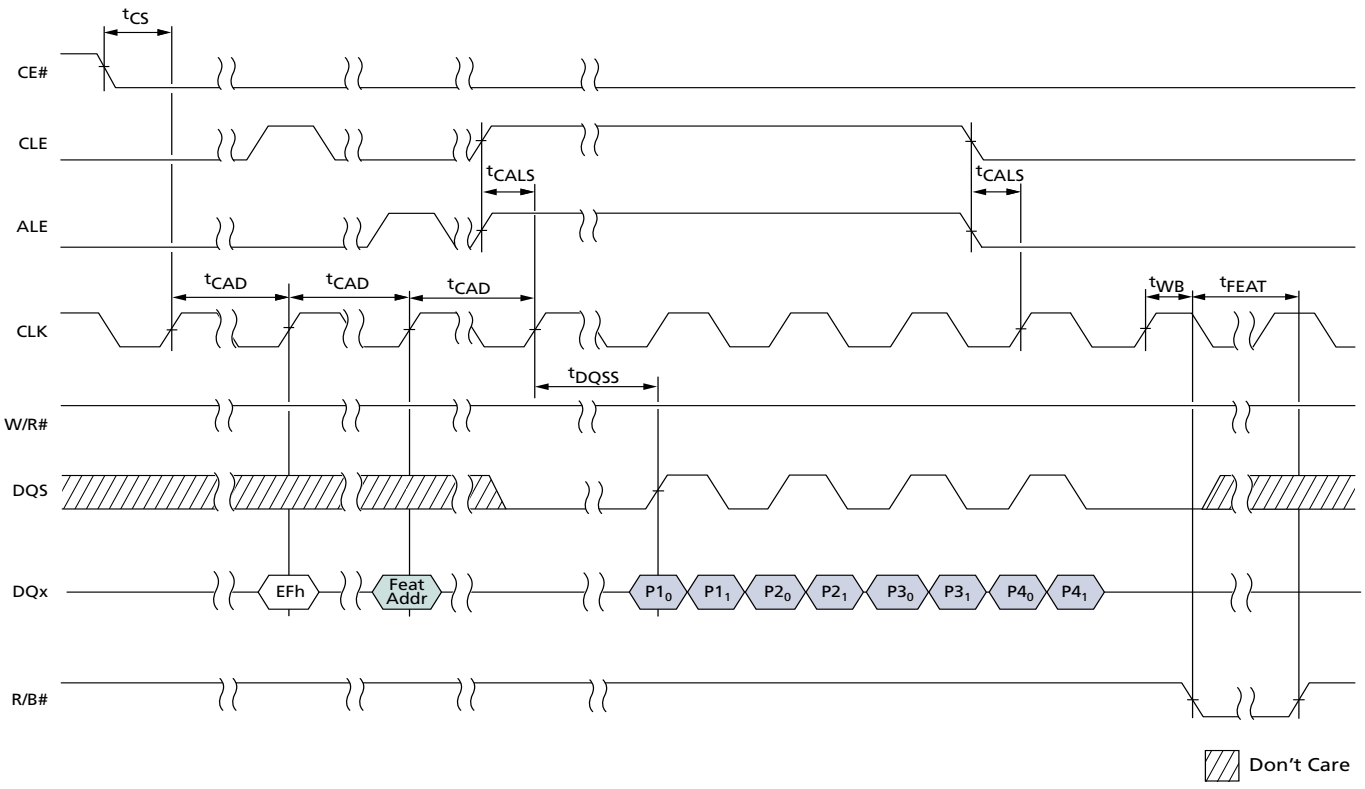


Figure 106: ERASE BLOCK Operation



NV-DDR Interface Timing Diagrams

Figure 107: SET FEATURES Operation



Notes:
1. When CE# remains LOW, tCAD begins at the rising edge of the clock from which the last data byte is input for the subsequent command or data input cycle(s).
2. tDSH (MIN) generally occurs during tDQSS (MIN).
3. tDSS (MIN) generally occurs during tDQSS (MAX).
4. The cycle that tCAD is measured from may be an idle cycle (as shown), another command cycle, an address cycle, or a data cycle. The idle cycle is shown in this diagram for simplicity.

Figure 108: READ ID Operation

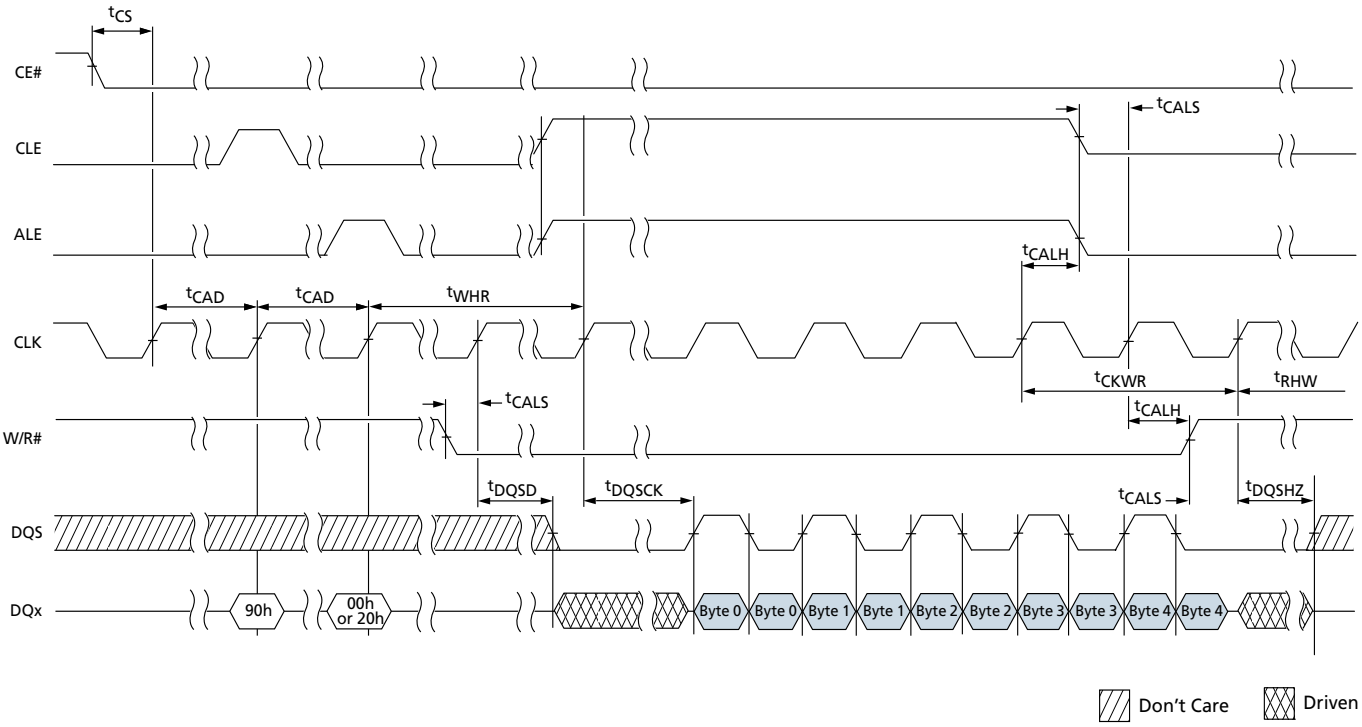


Figure 109: GET FEATURES Operation

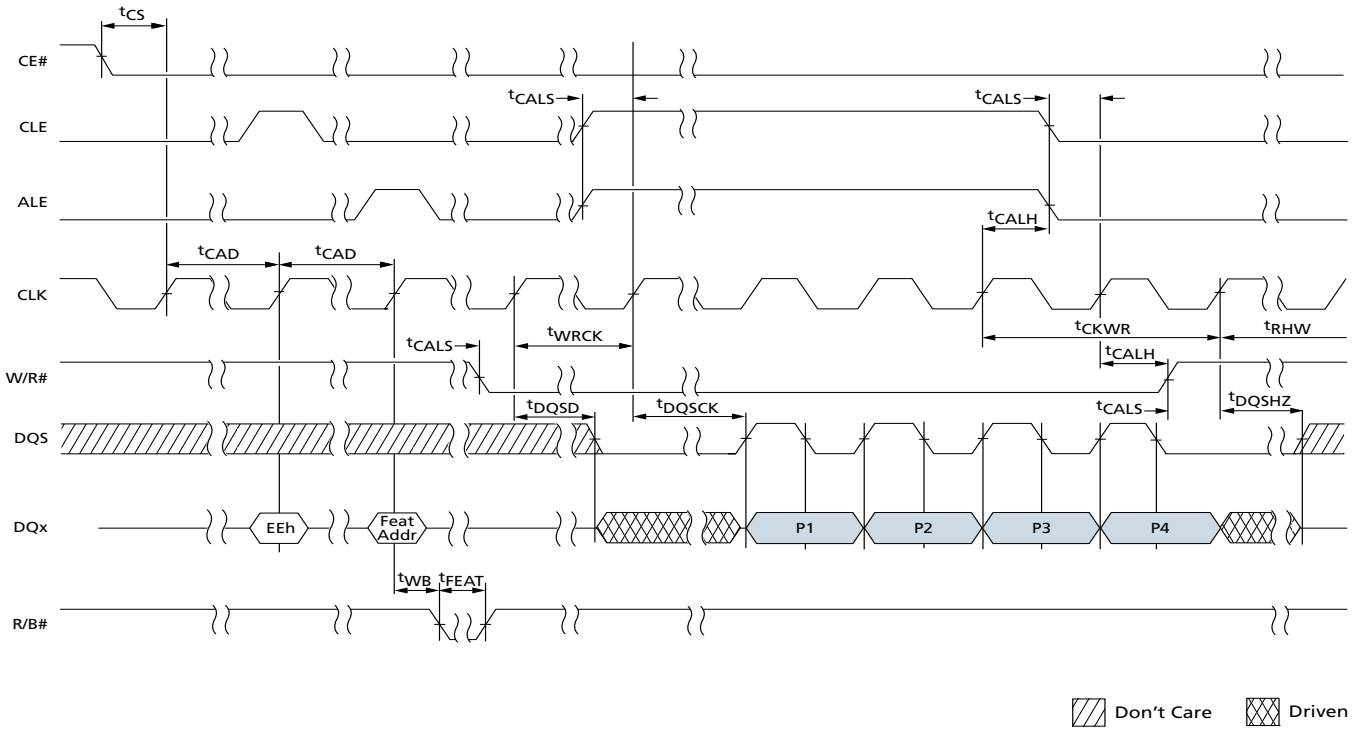


Figure 110: RESET (FCh) Operation

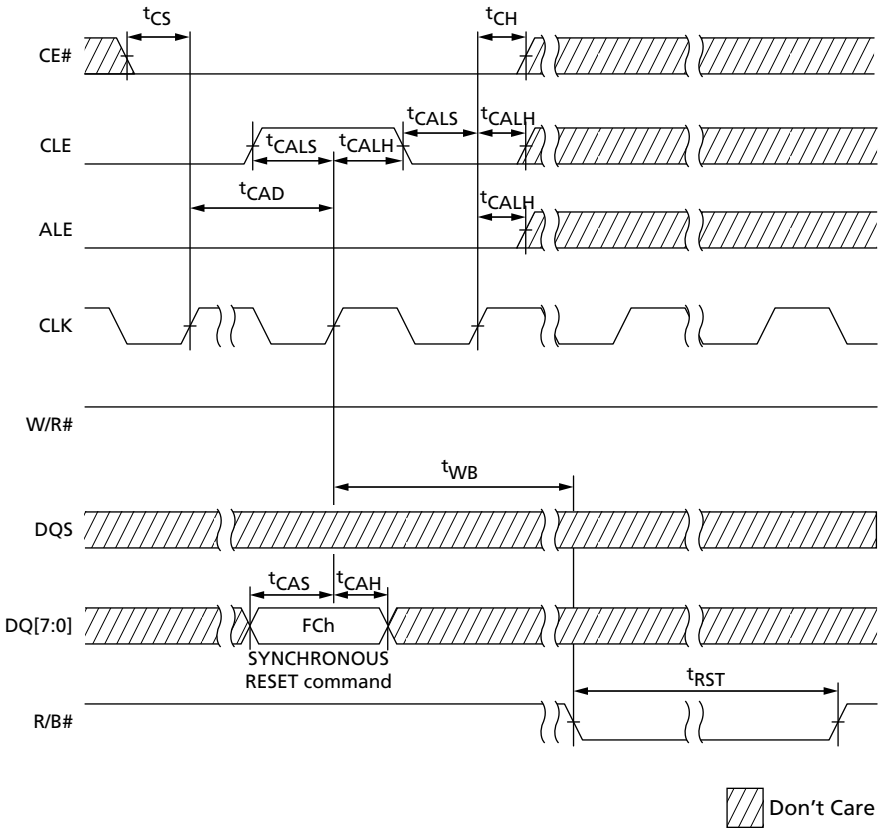


Figure 111: READ STATUS Cycle

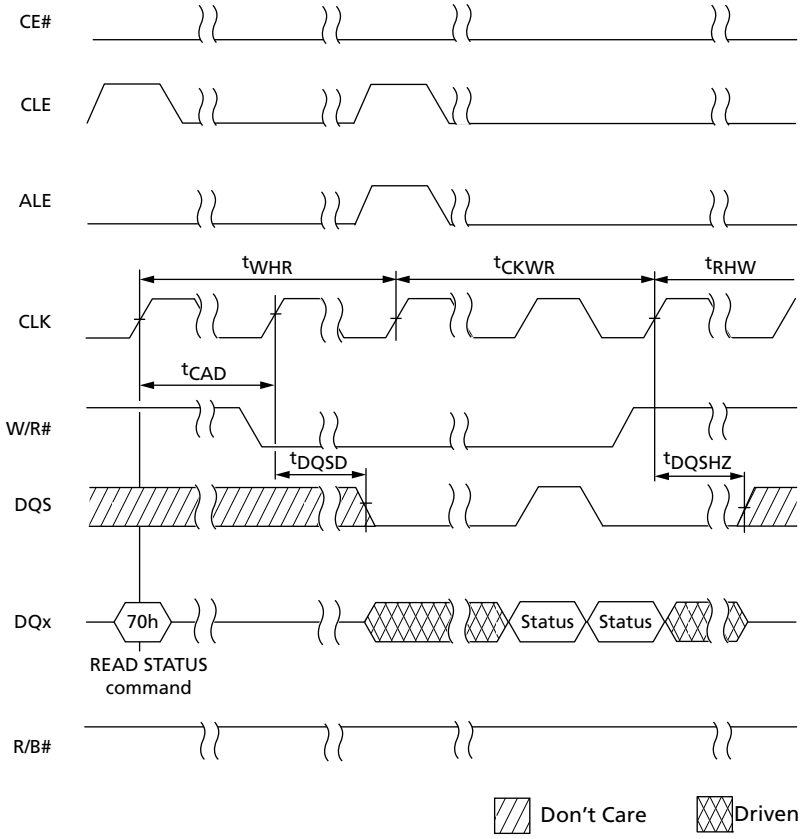


Figure 112: READ STATUS ENHANCED Operation

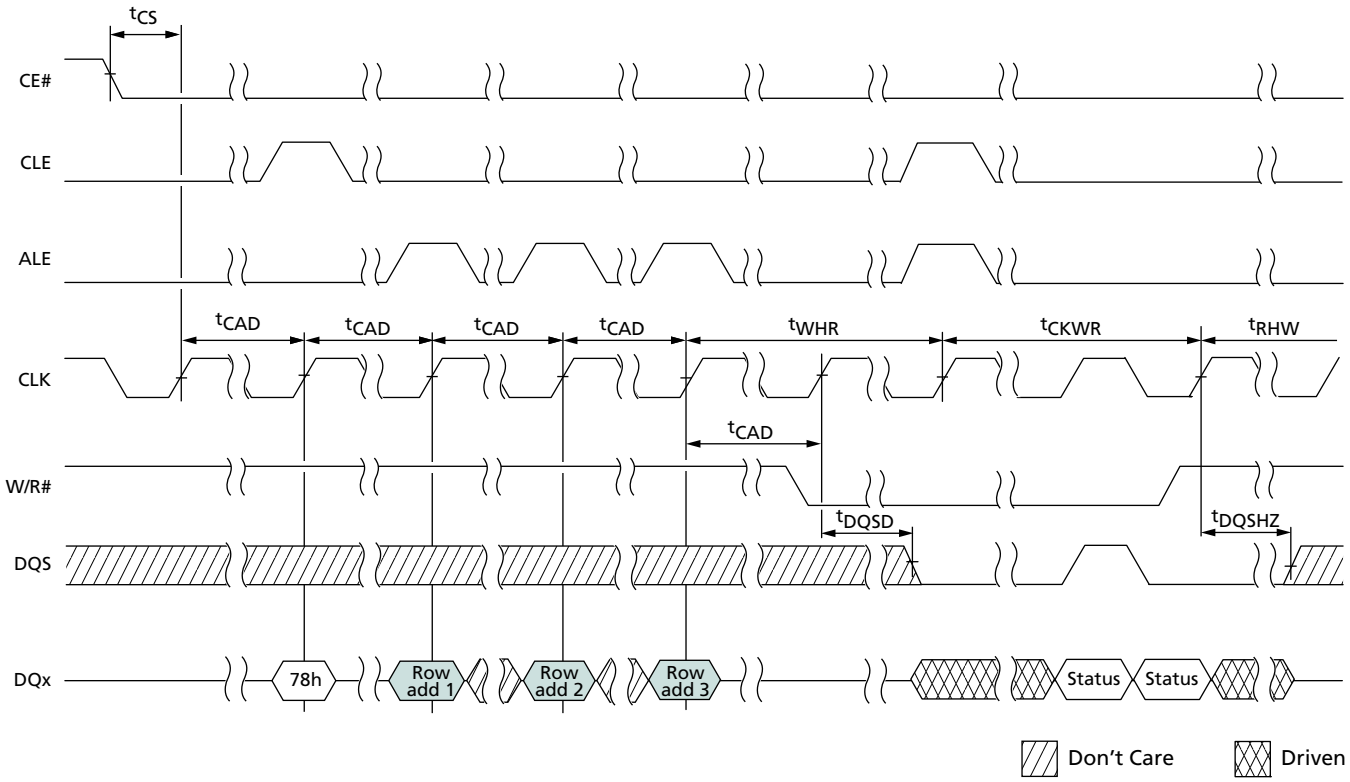


Figure 113: READ PARAMETER PAGE Operation

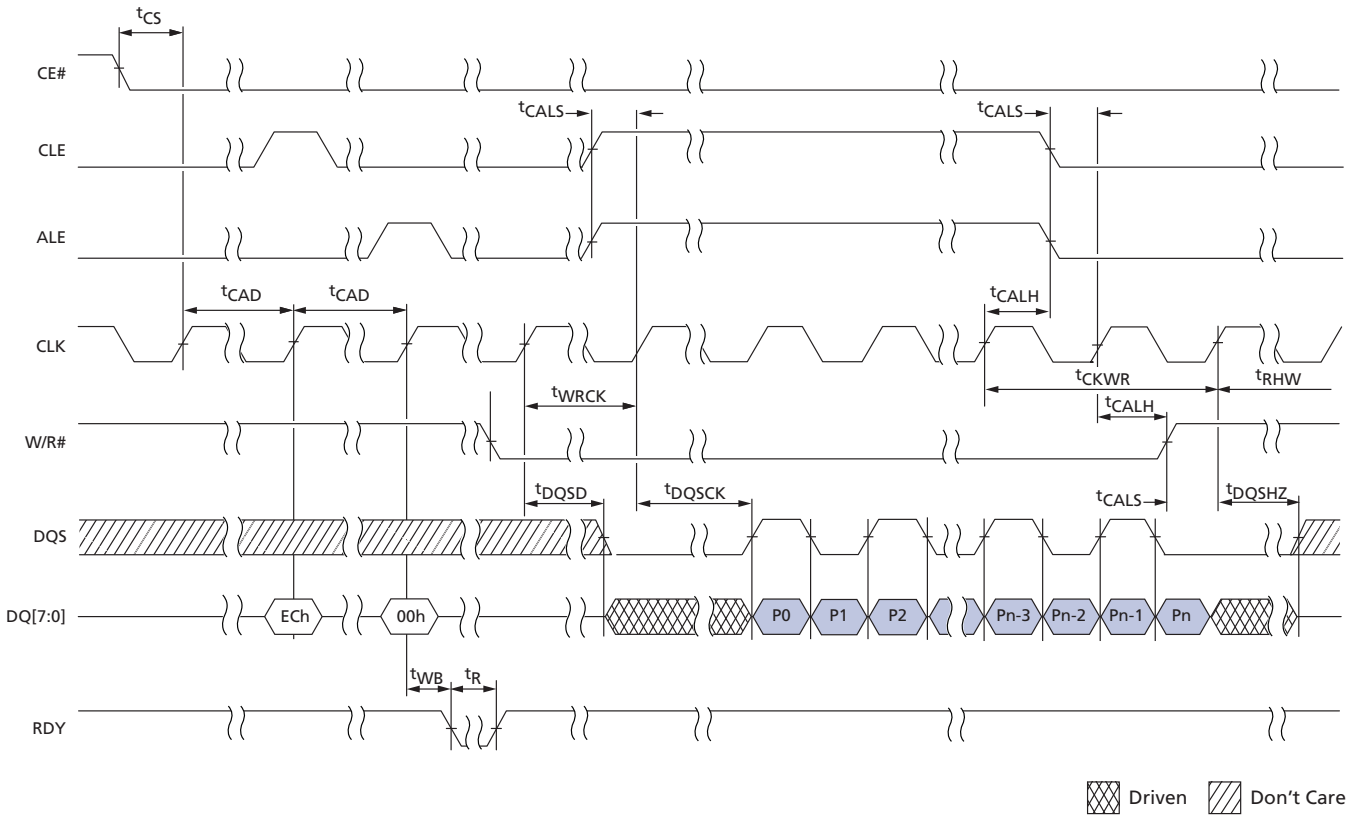


Figure 114: READ PAGE Operation

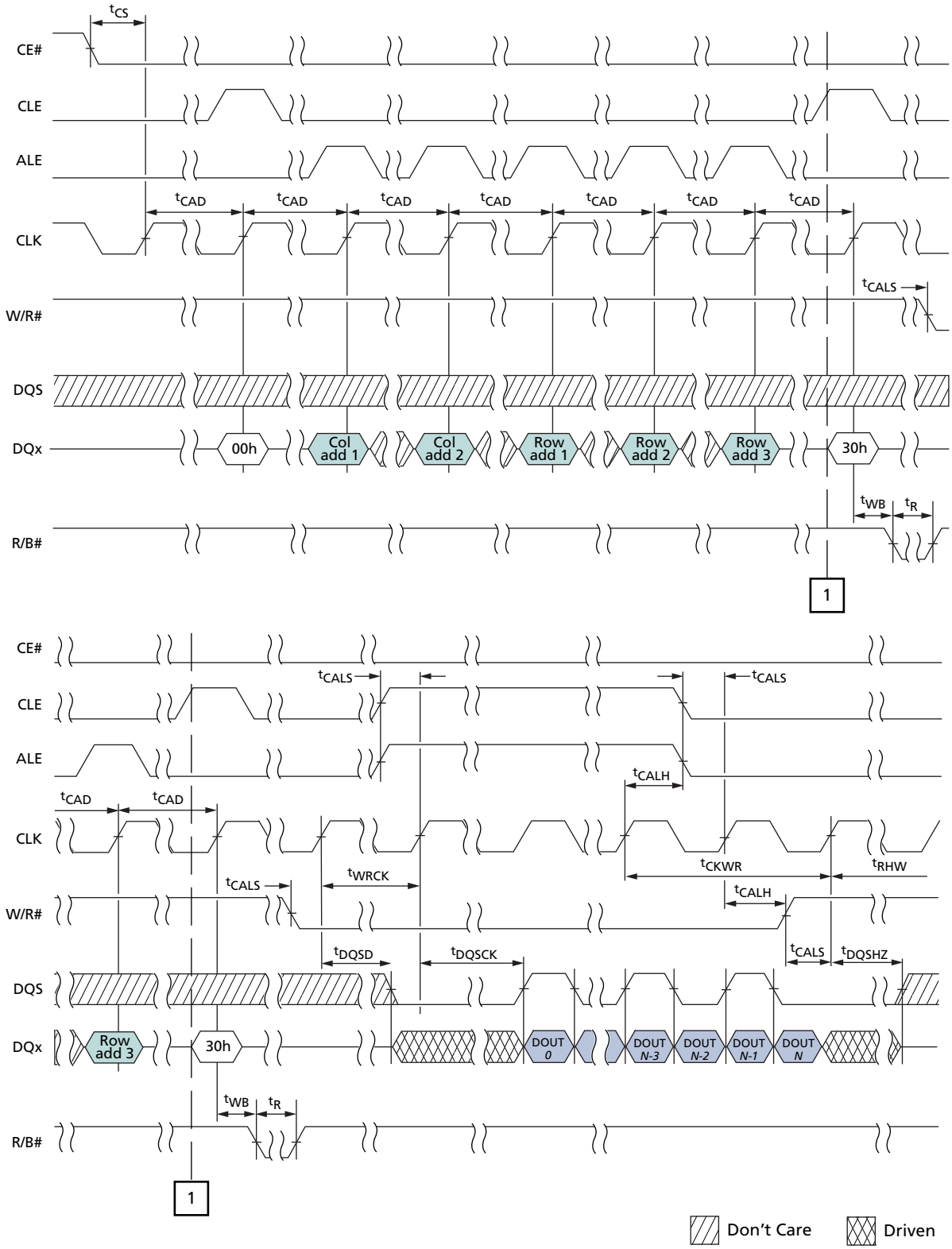


Figure 115: CHANGE READ COLUMN

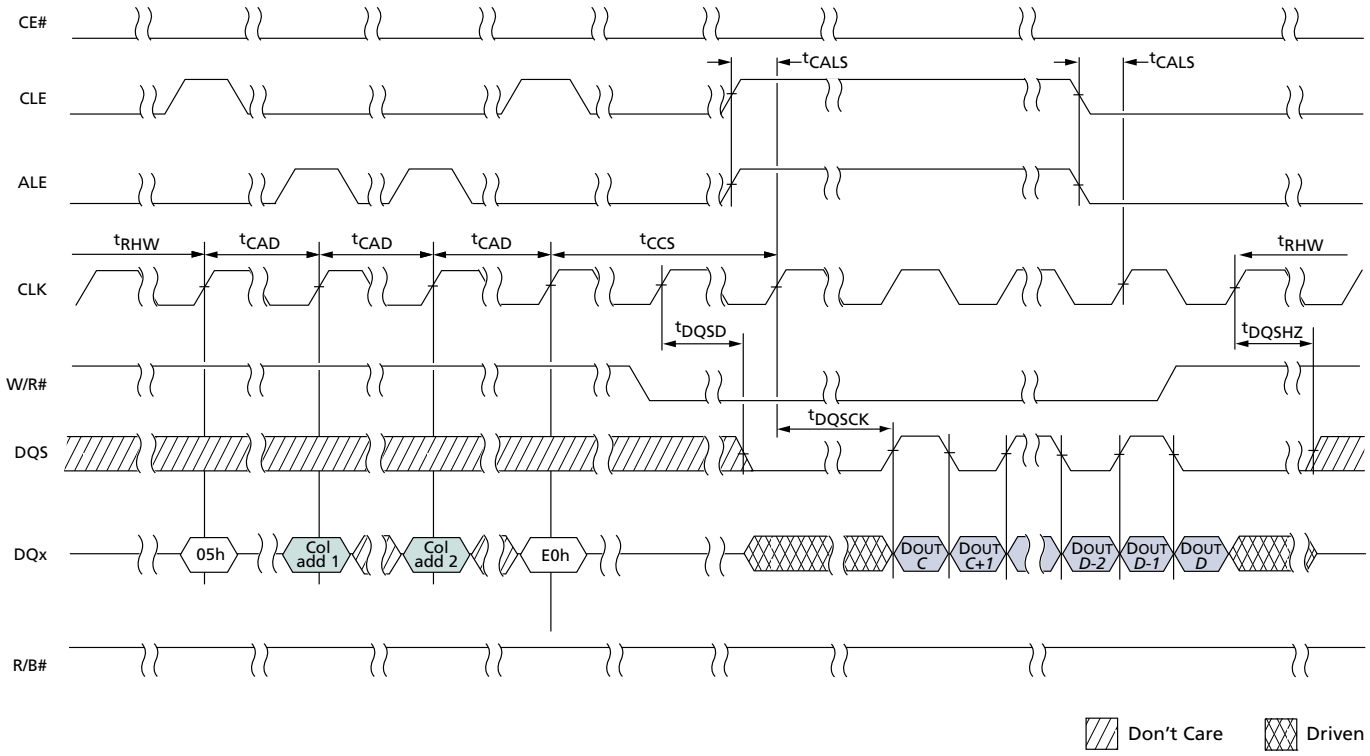


Figure 116: Multi-Plane Read Page (1 of 2)

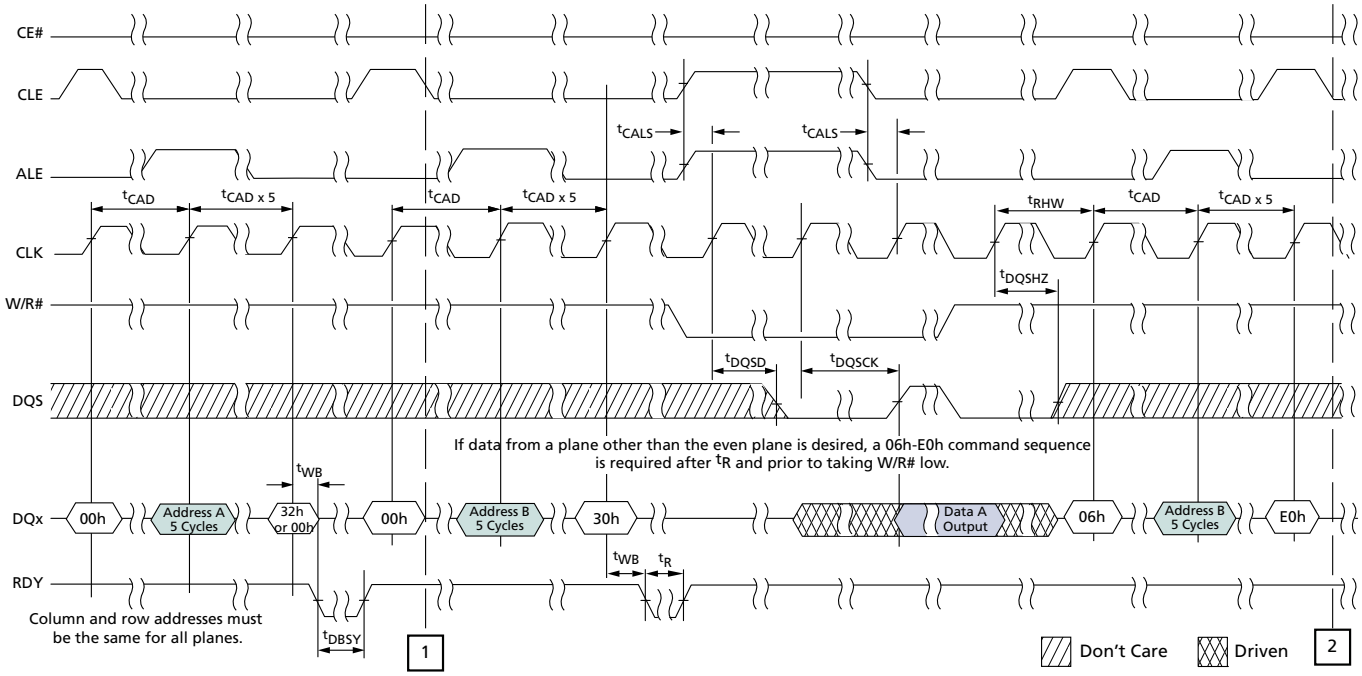


Figure 117: Multi-Plane Read Page (2 of 2)

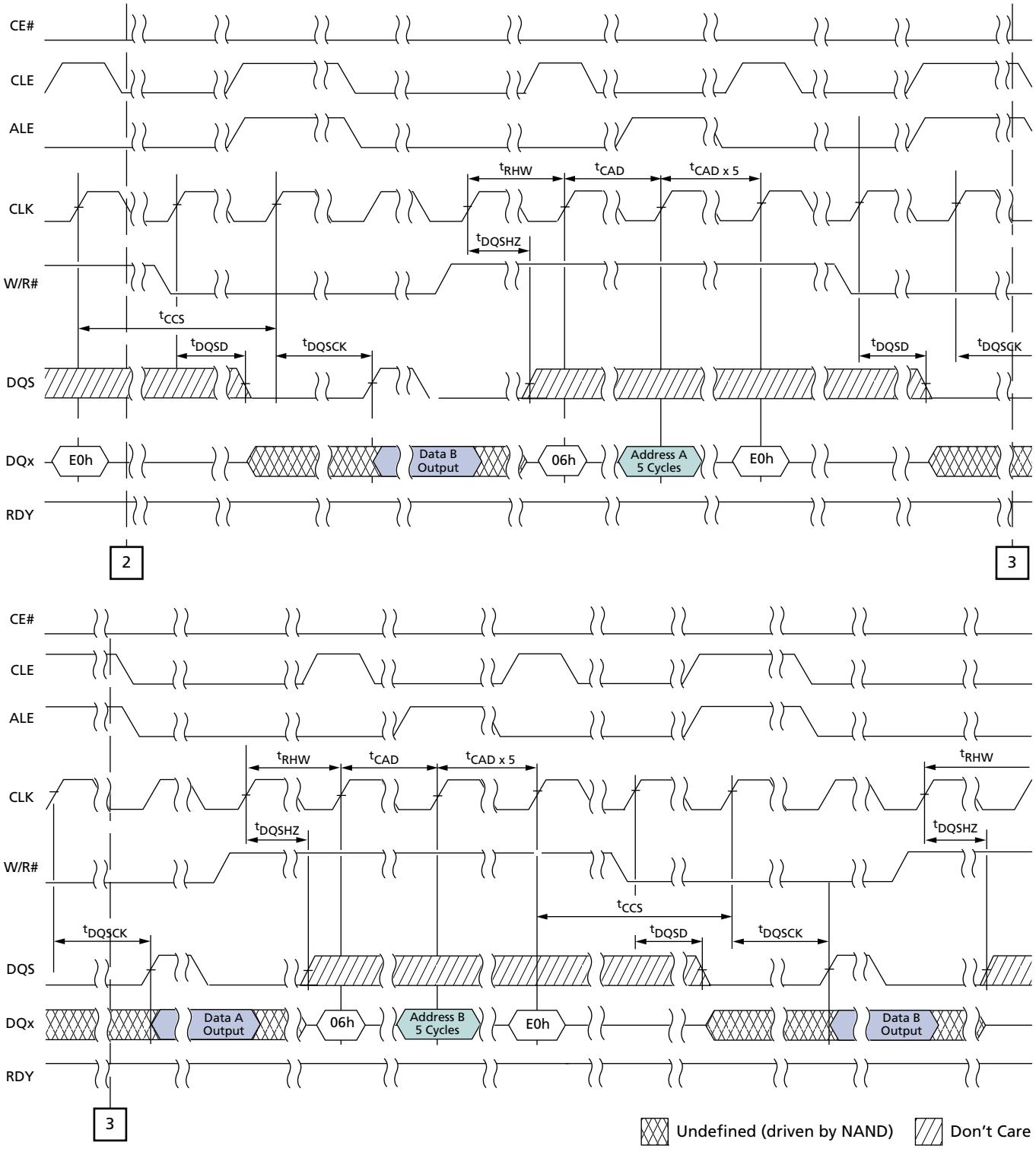
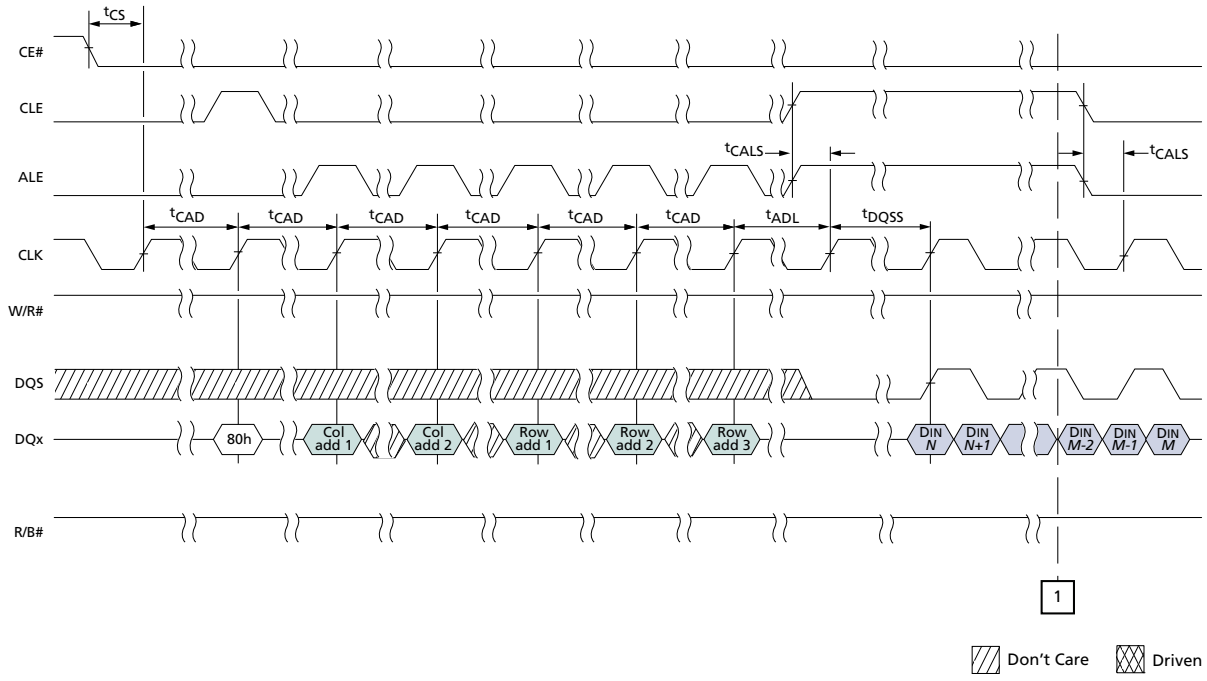
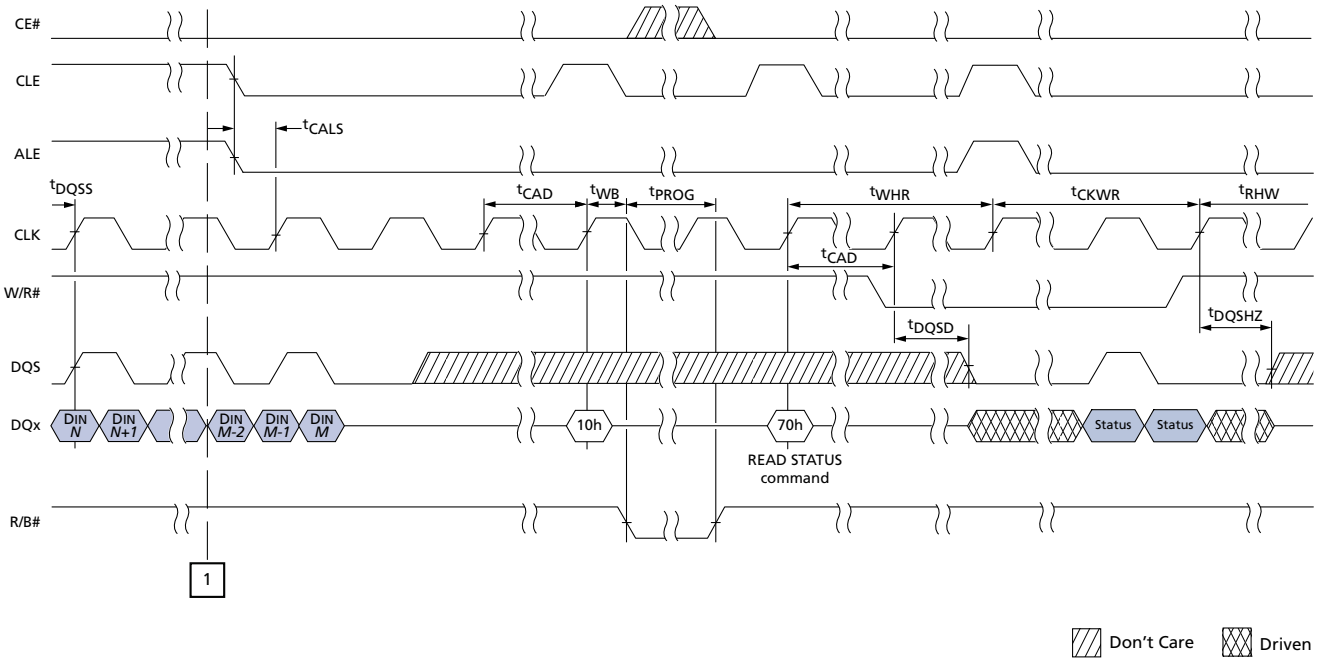


Figure 118: PROGRAM PAGE Operation (1 of 2)



Note: Programming timing figures do not represent single-pass programming format - to be updated.

Figure 119: PROGRAM PAGE Operation (2 of 2)



Note: Programming timing figures do not represent single-pass programming format - to be updated.

Figure 120: CHANGE WRITE COLUMN

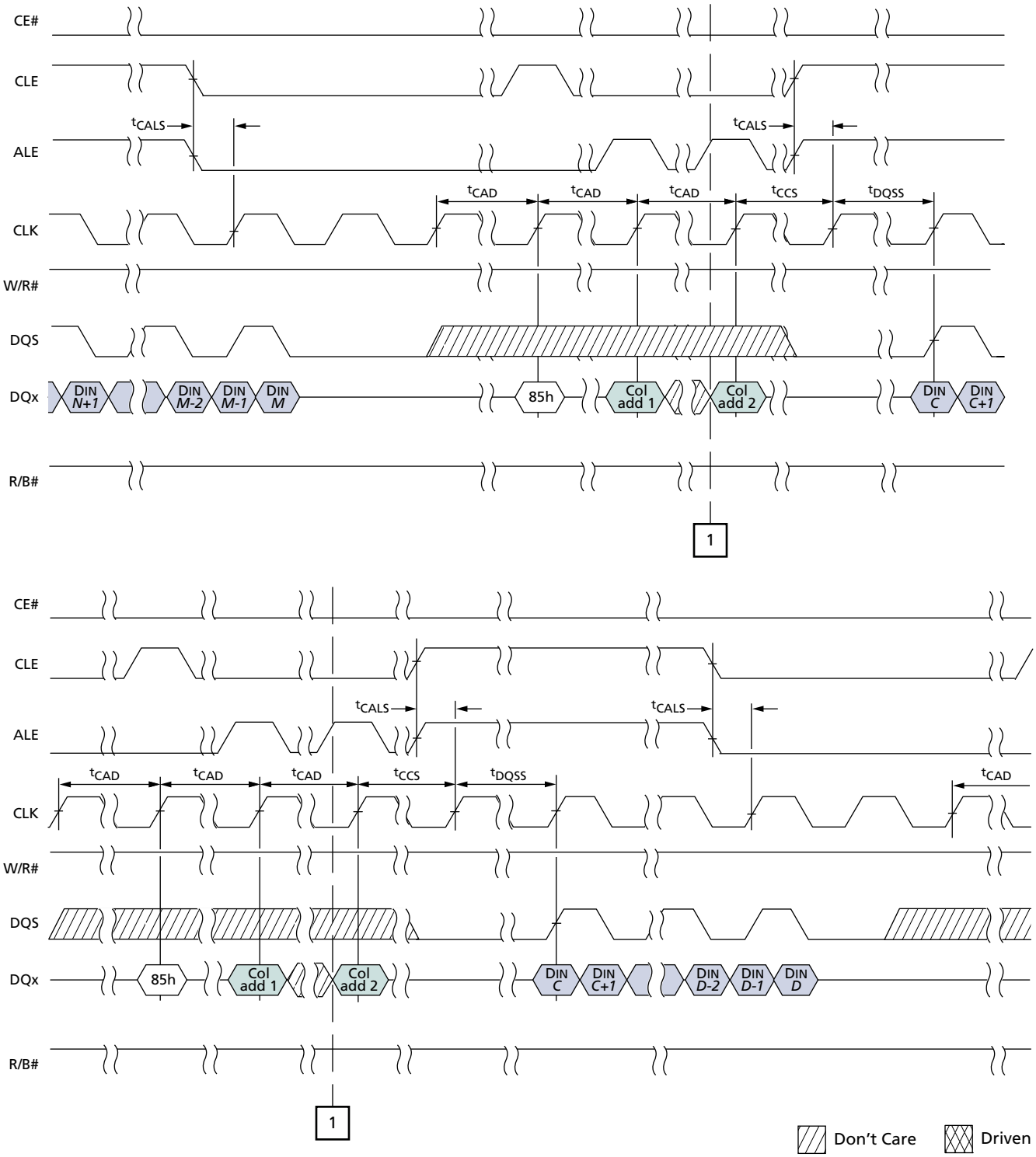
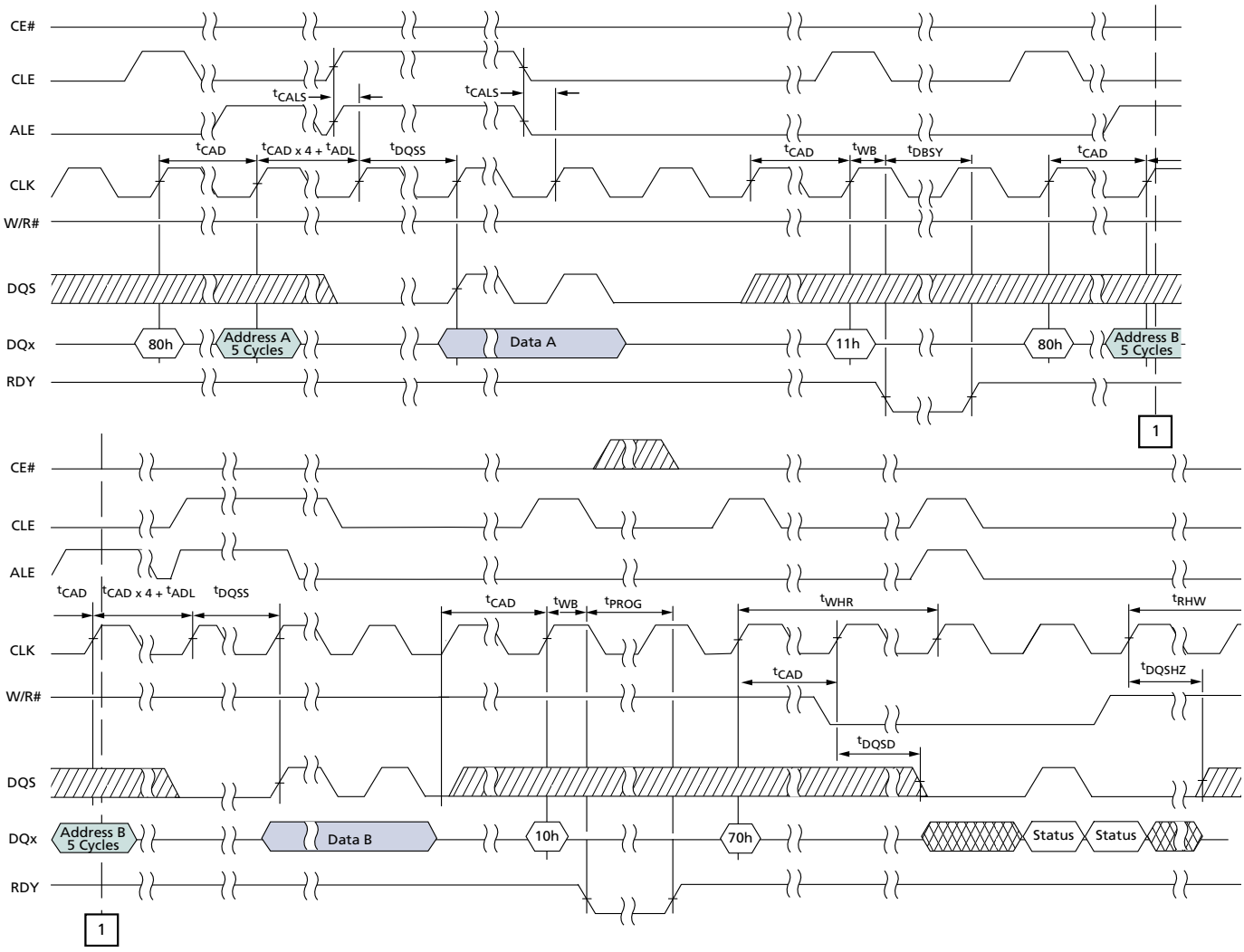


Figure 121: Multi-Plane Program Page



Note: Programming timing figures do not represent single-pass programming format - to be updated.

Figure 122: ERASE BLOCK

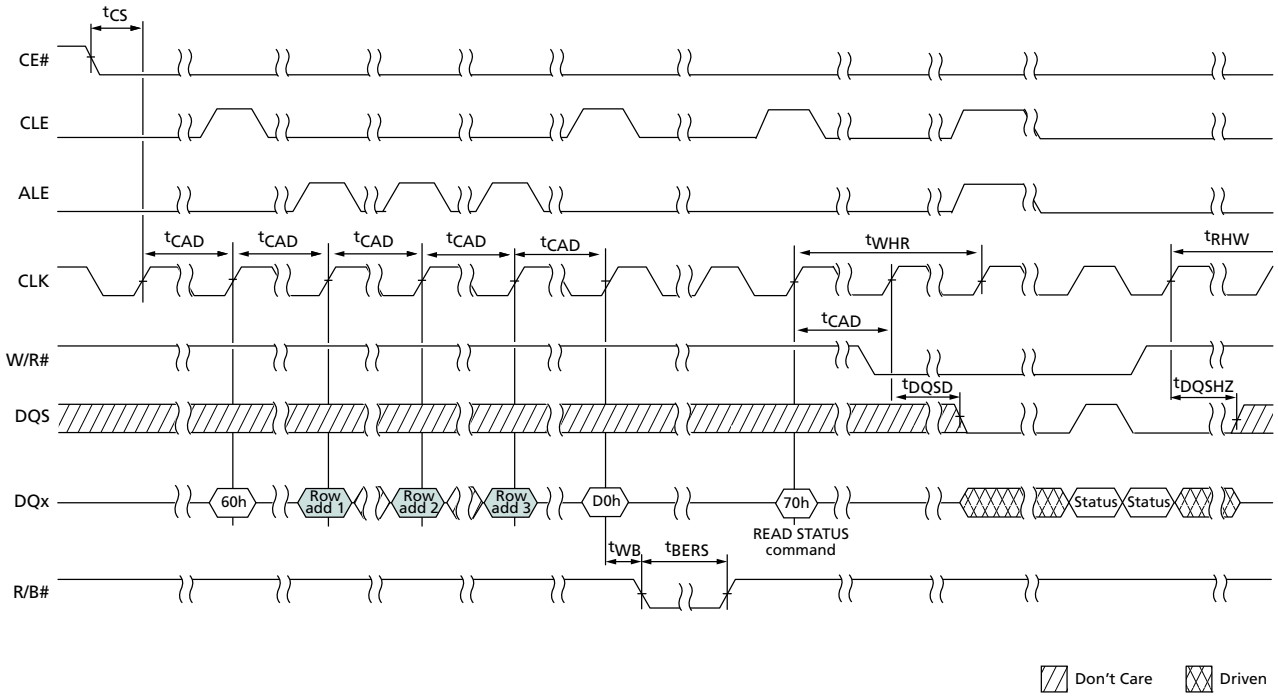


Figure 123: COPYBACK (1 of 3)

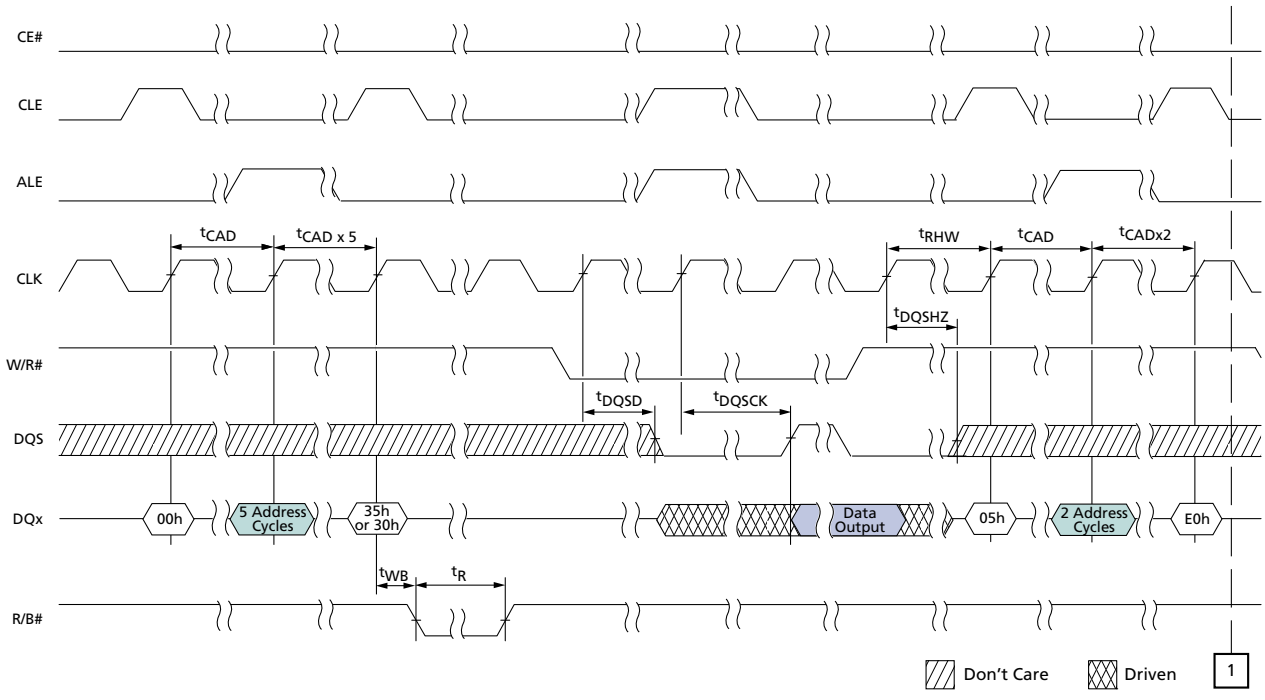
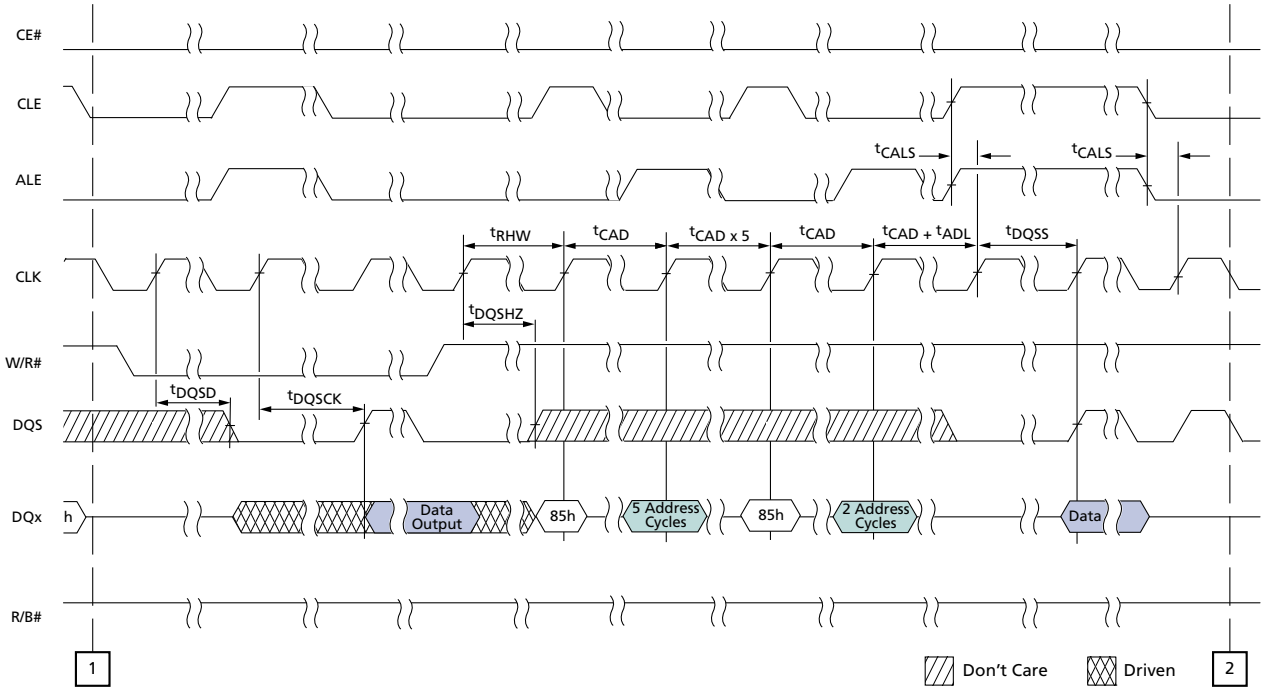
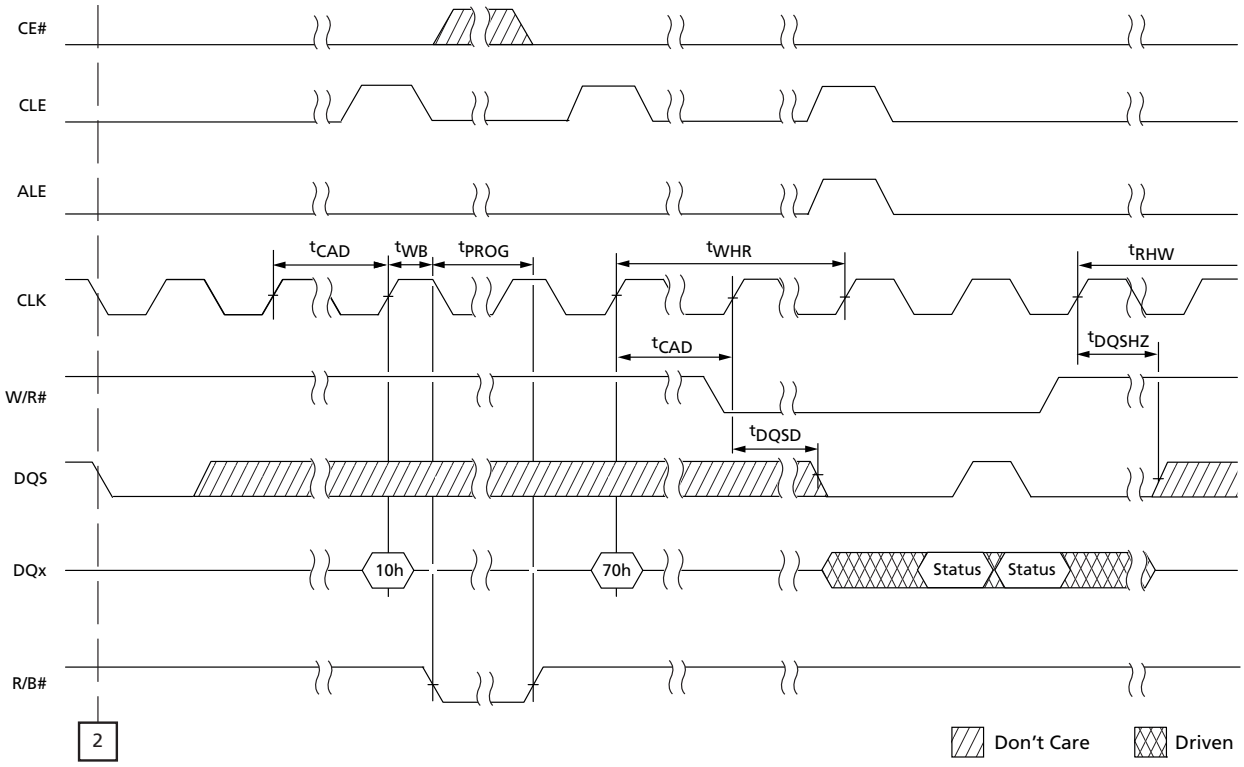


Figure 124: COPYBACK (2 of 3)



Note: Programming timing figures do not represent single-pass programming format - to be updated.

Figure 125: COPYBACK (3 of 3)



Note: Programming timing figures do not represent single-pass programming format - to be updated.

NV-DDR2 Interface Timing Diagrams

Figure 126: SET FEATURES Operation

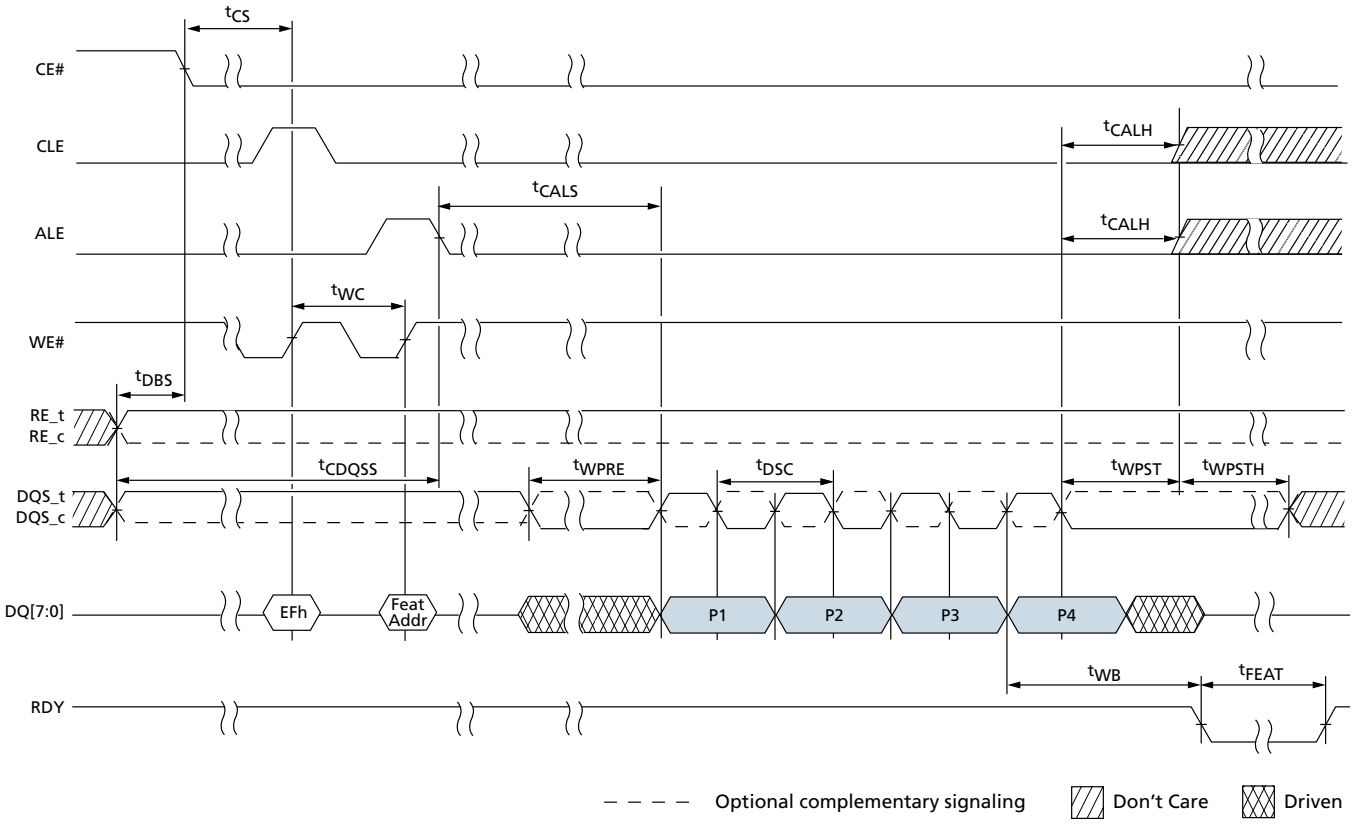


Figure 127: READ ID Operation

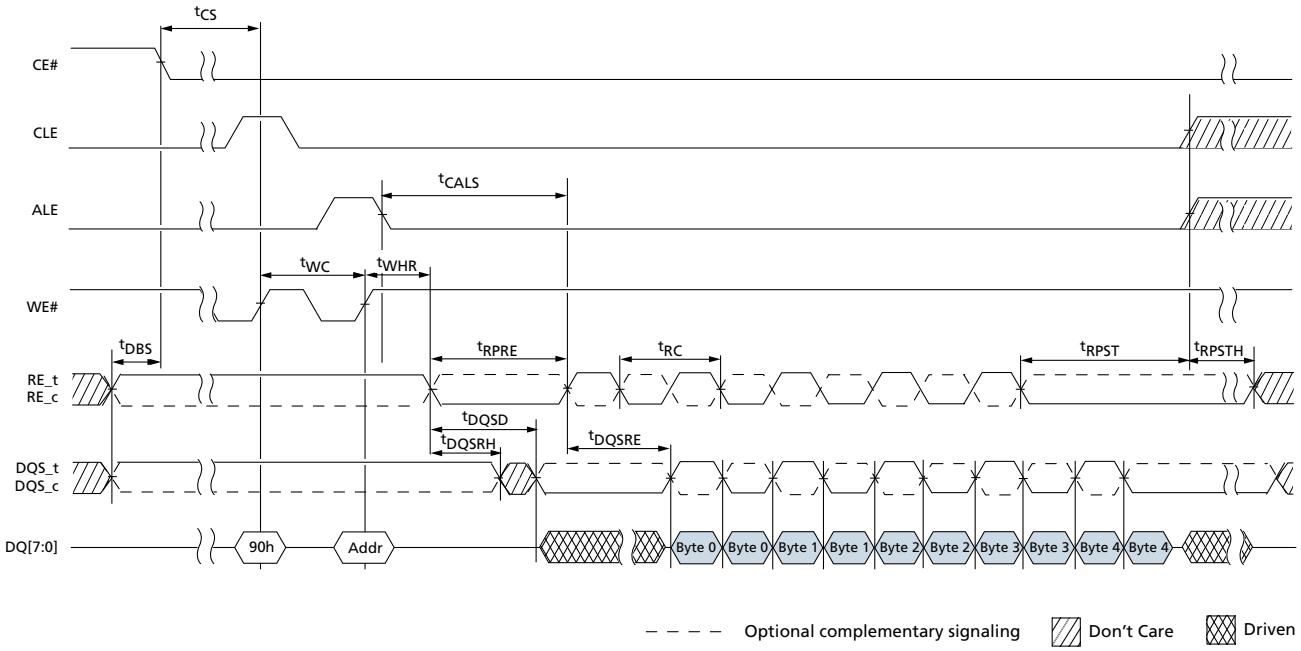


Figure 128: GET FEATURES Operation

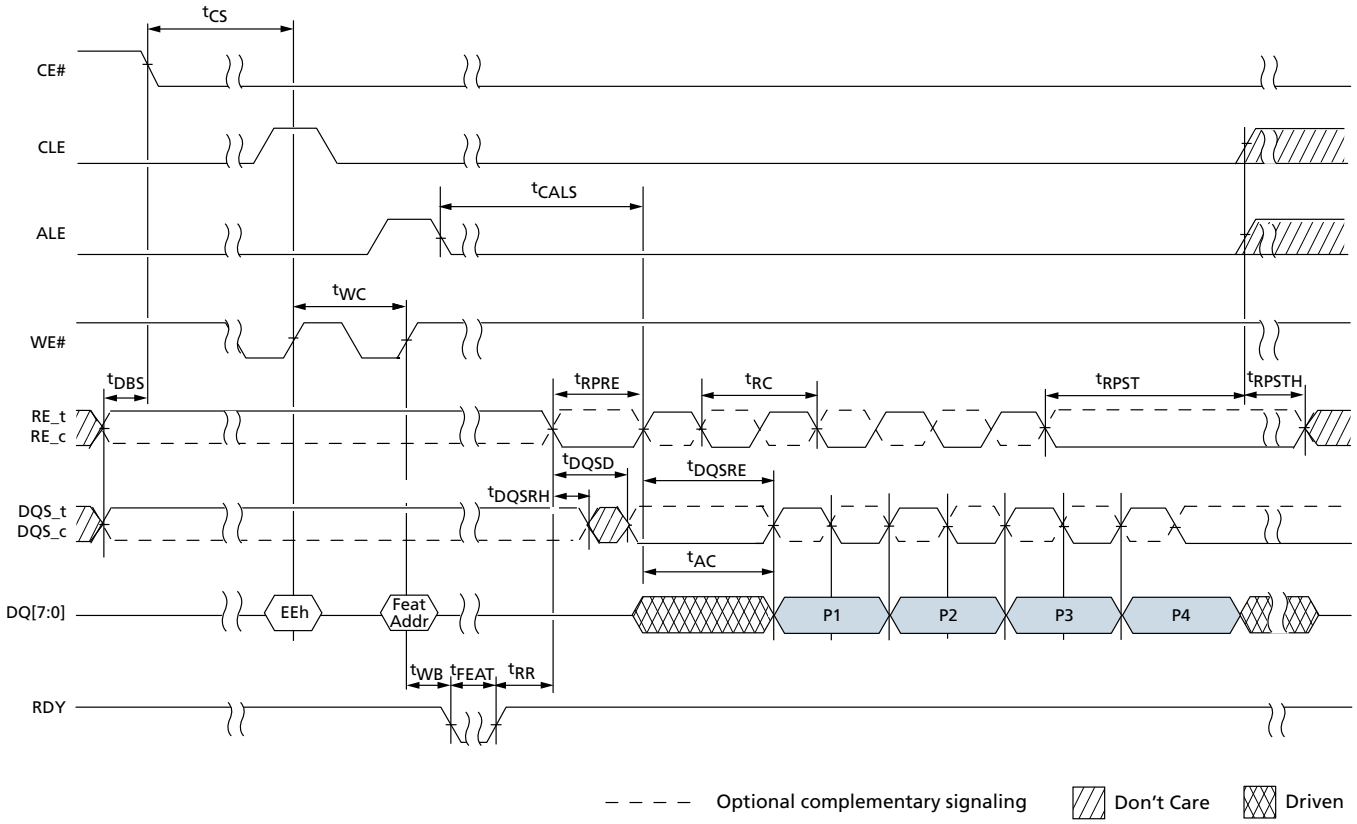


Figure 129: RESET (FCh) Operation

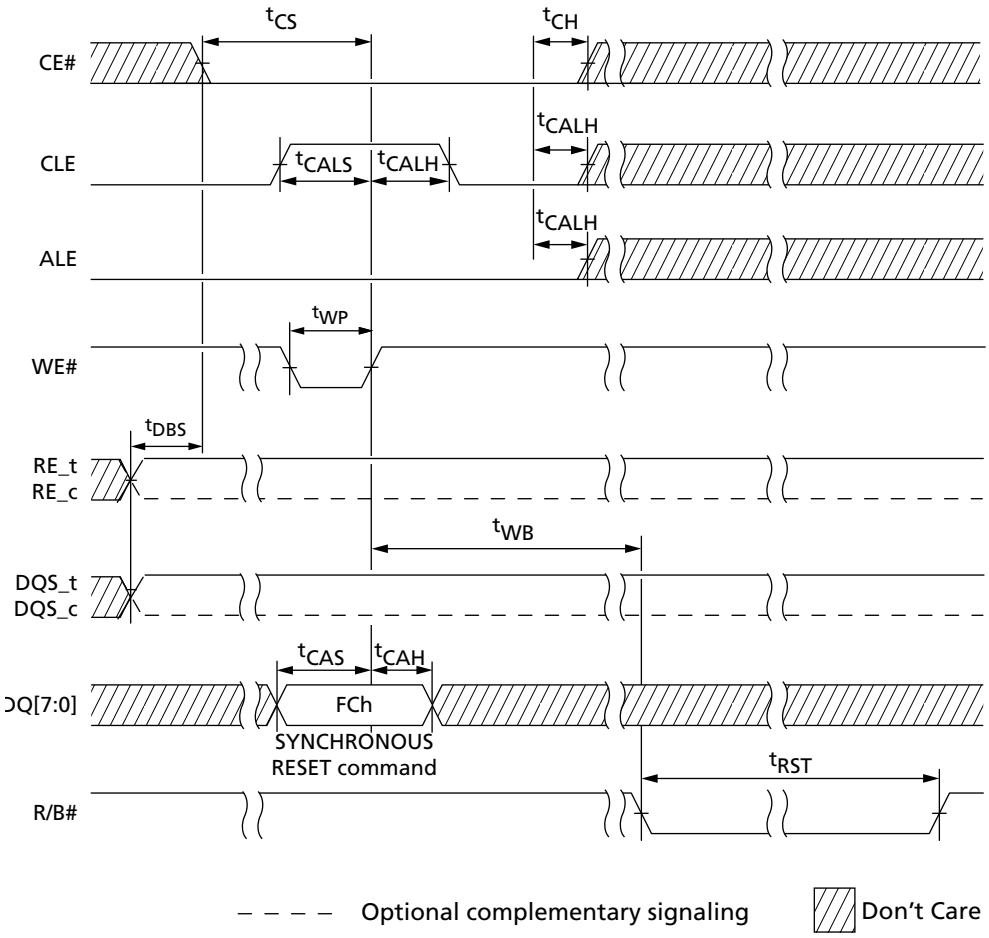


Figure 130: READ STATUS Cycle

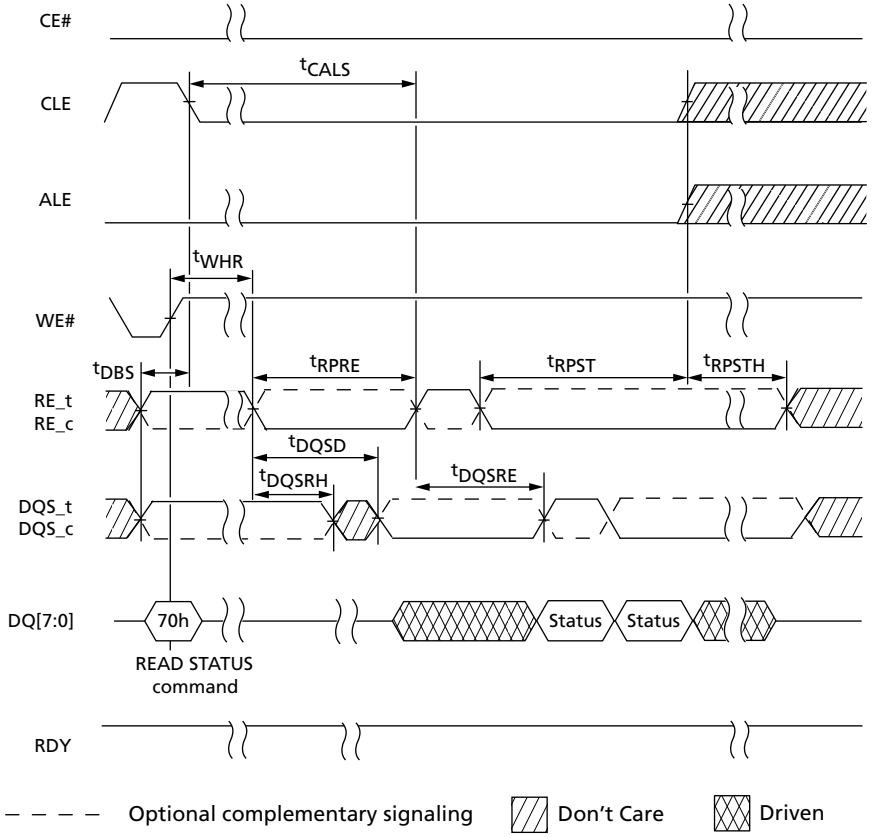


Figure 131: READ STATUS ENHANCED Operation

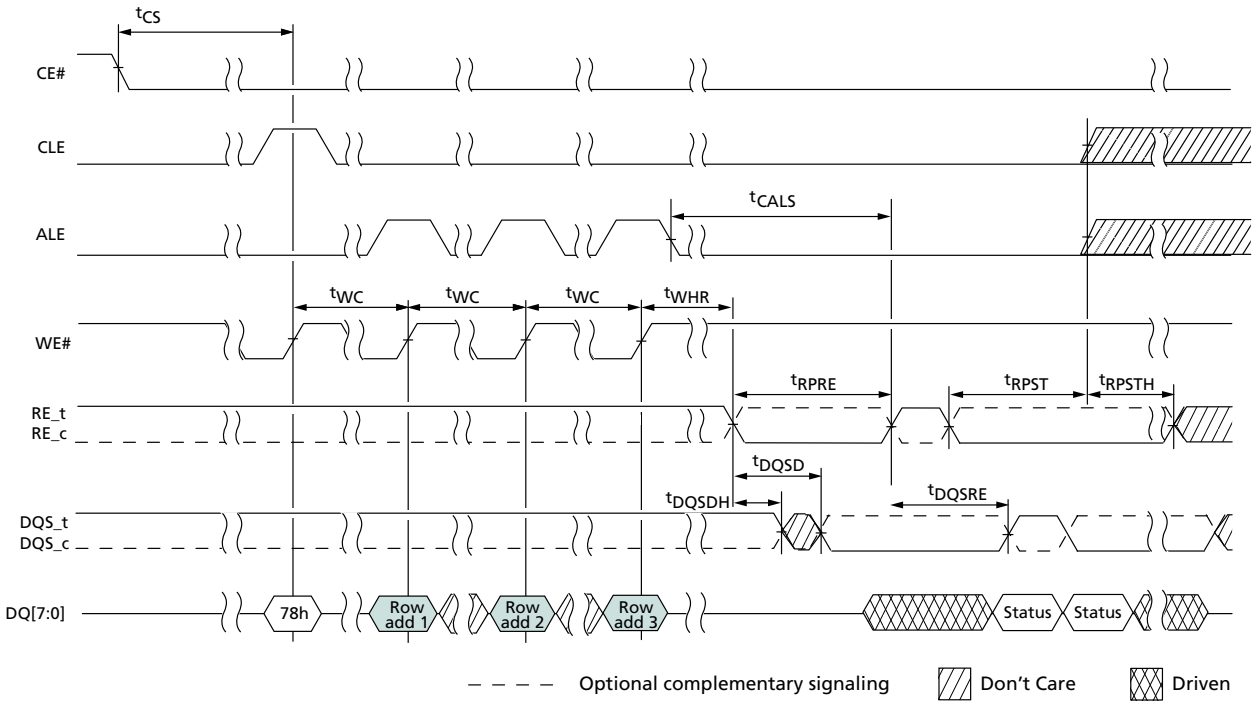


Figure 132: READ PARAMETER PAGE Operation

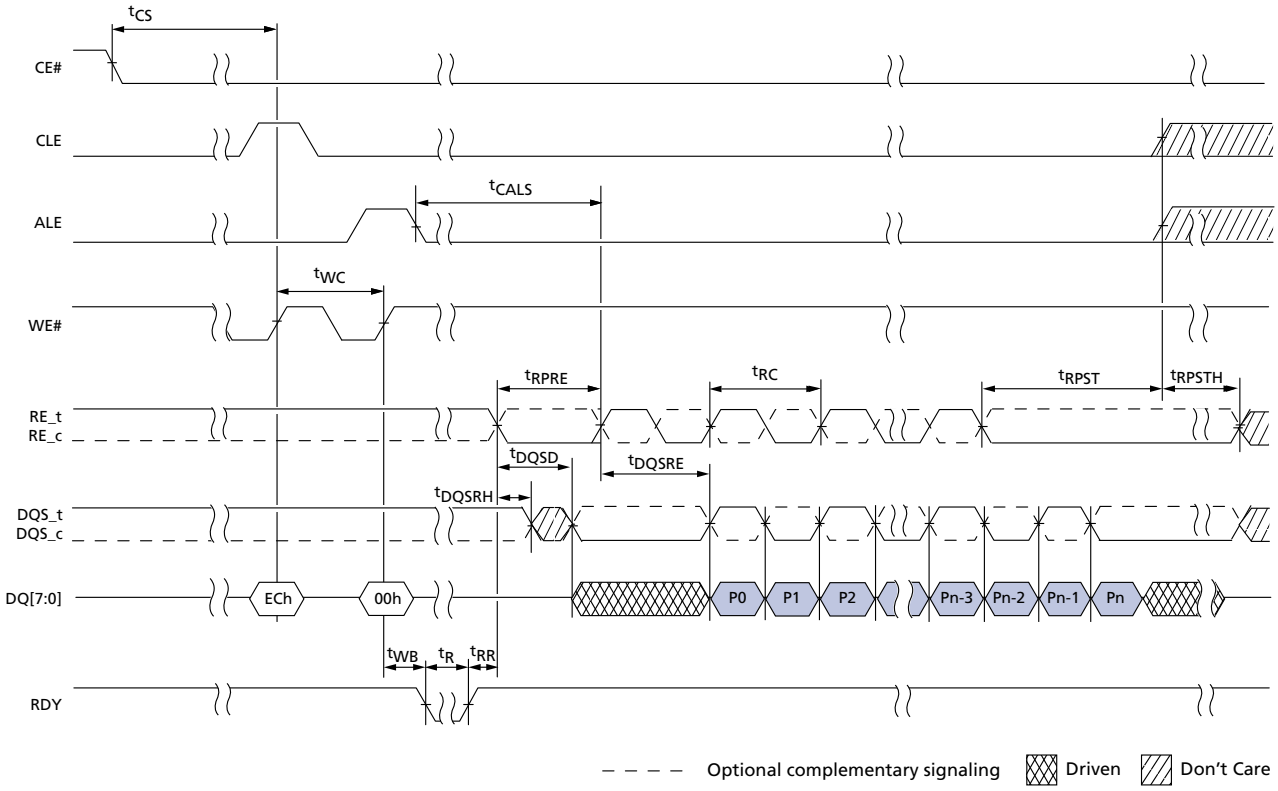


Figure 133: READ PAGE Operation

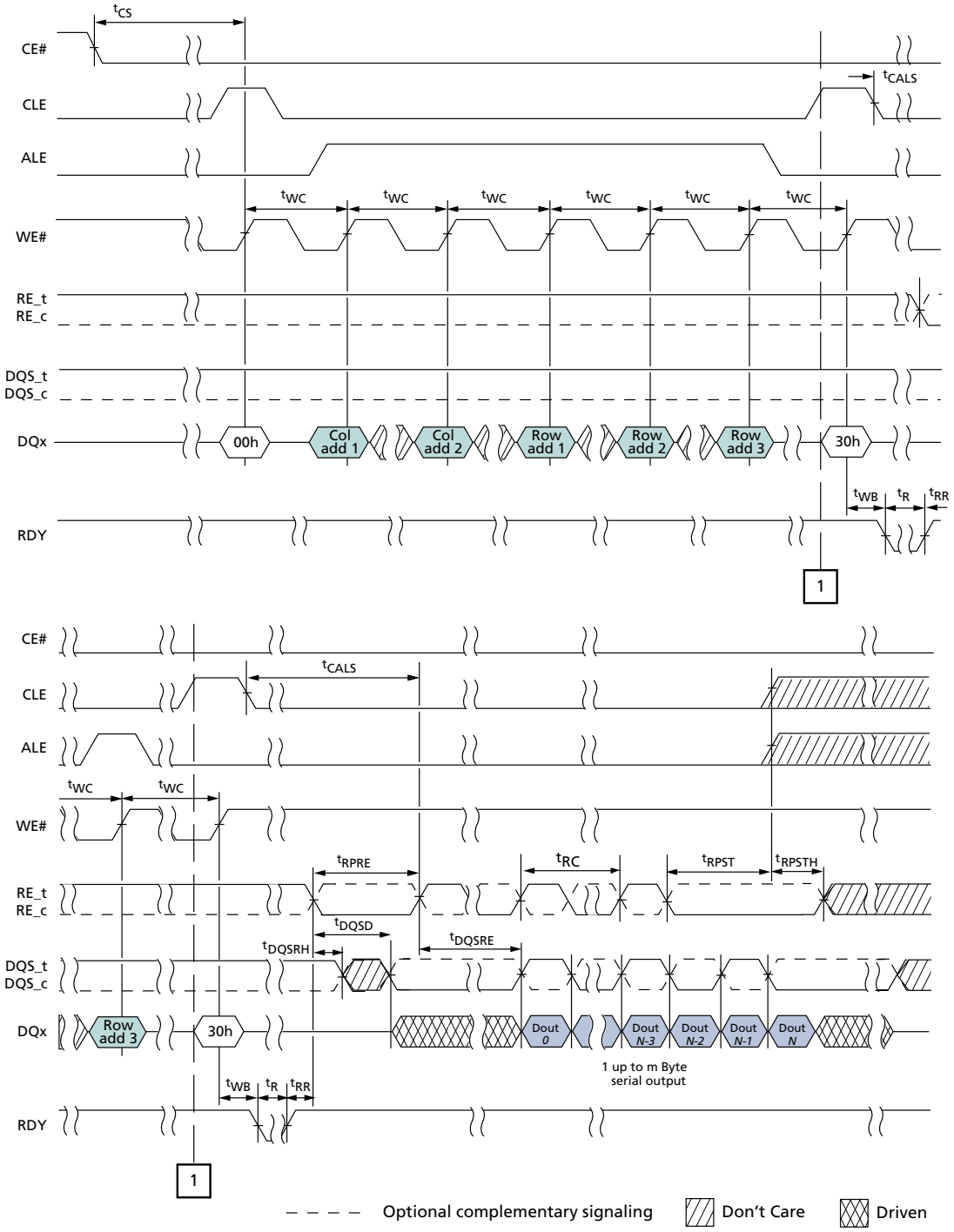


Figure 134: CHANGE READ COLUMN

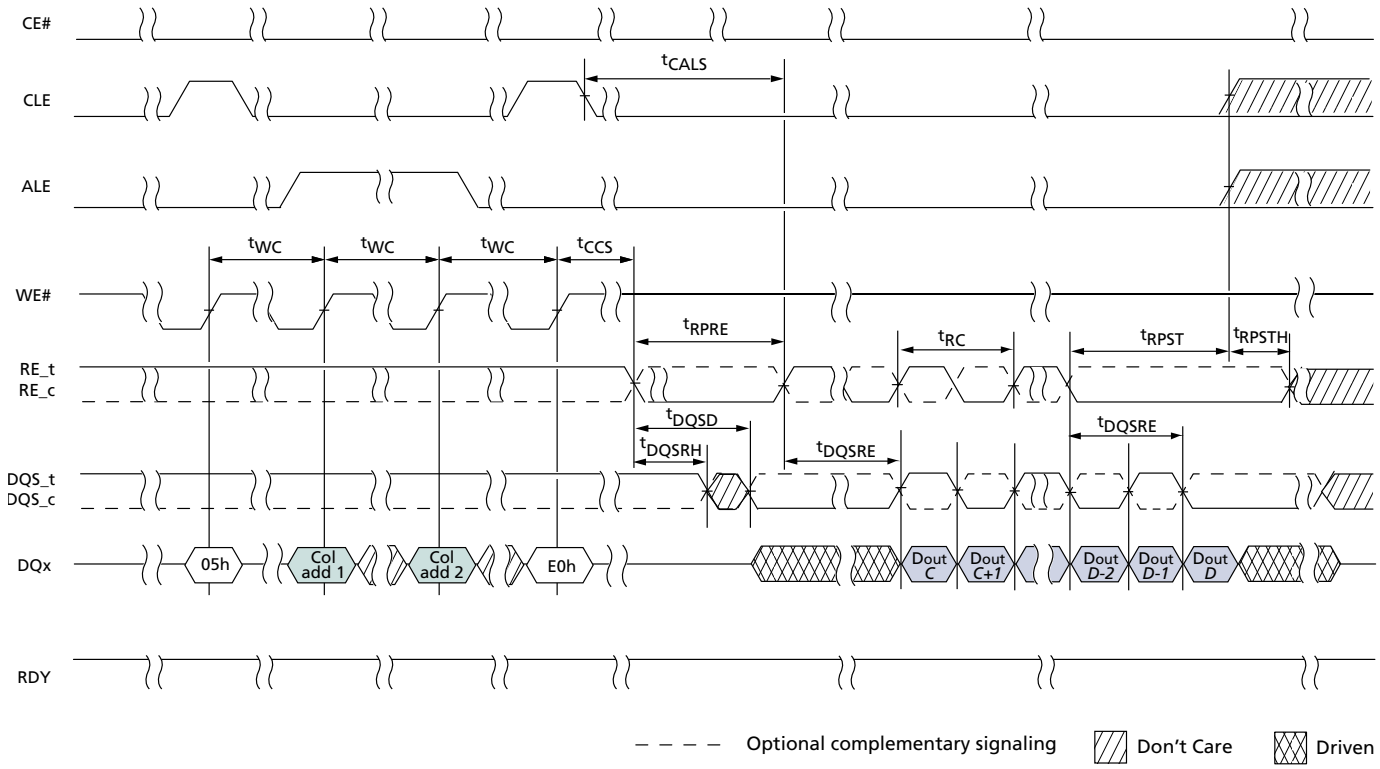


Figure 135: Multi-Plane Read Page (1 of 2)

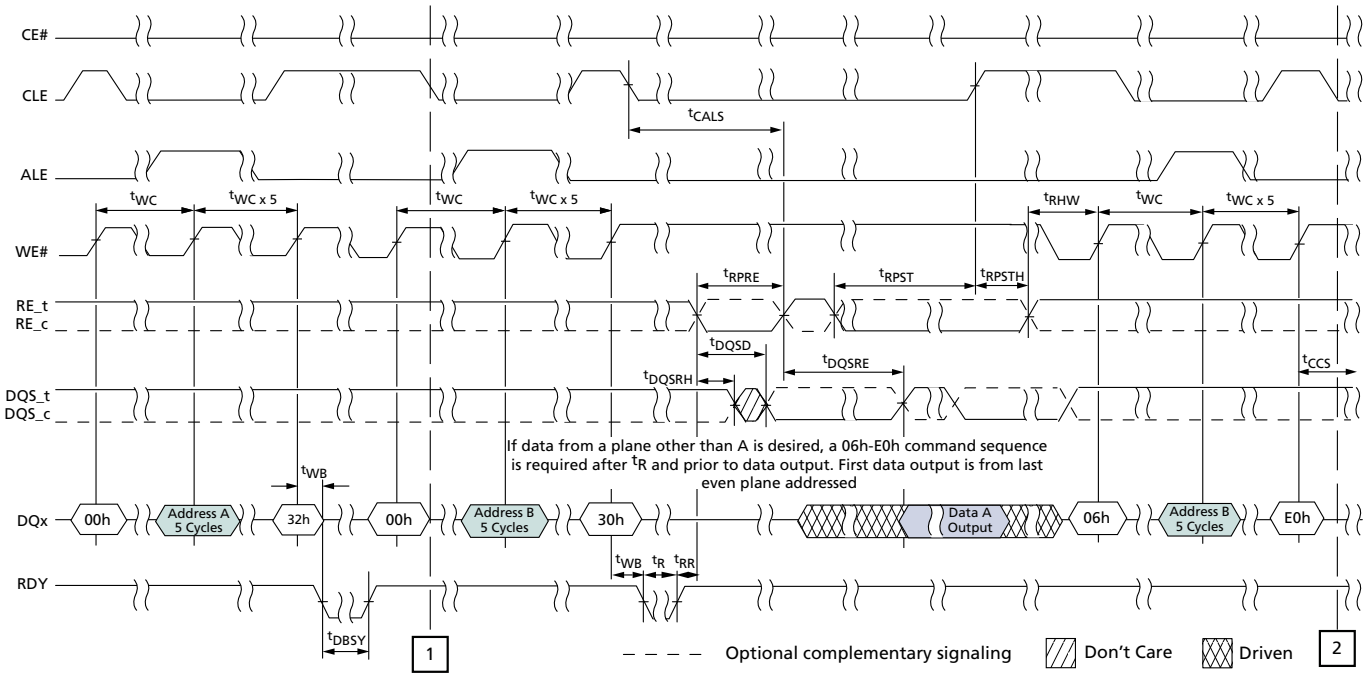


Figure 136: Multi-Plane Read Page (2 of 2)

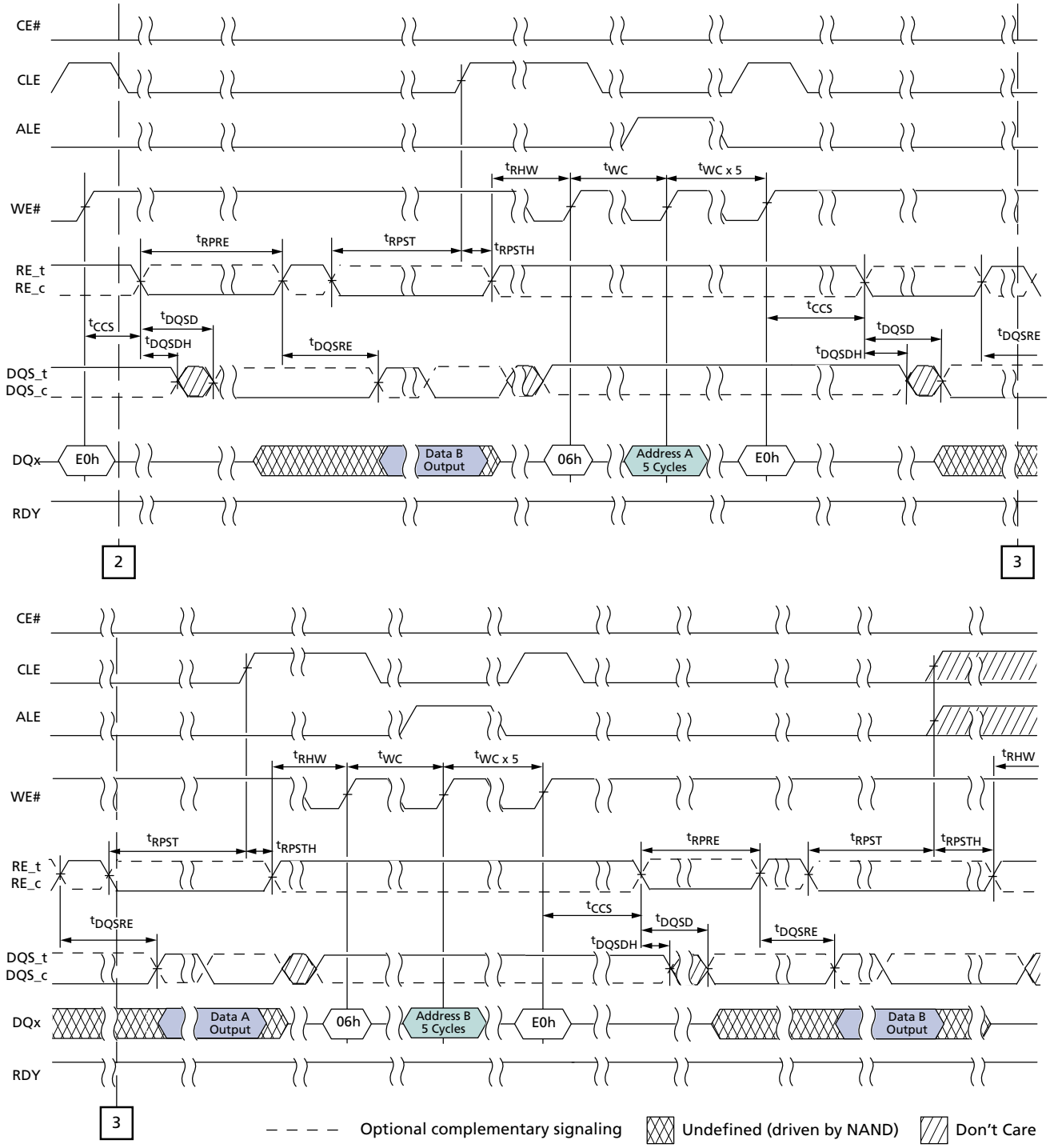


Figure 137: CHANGE WRITE COLUMN

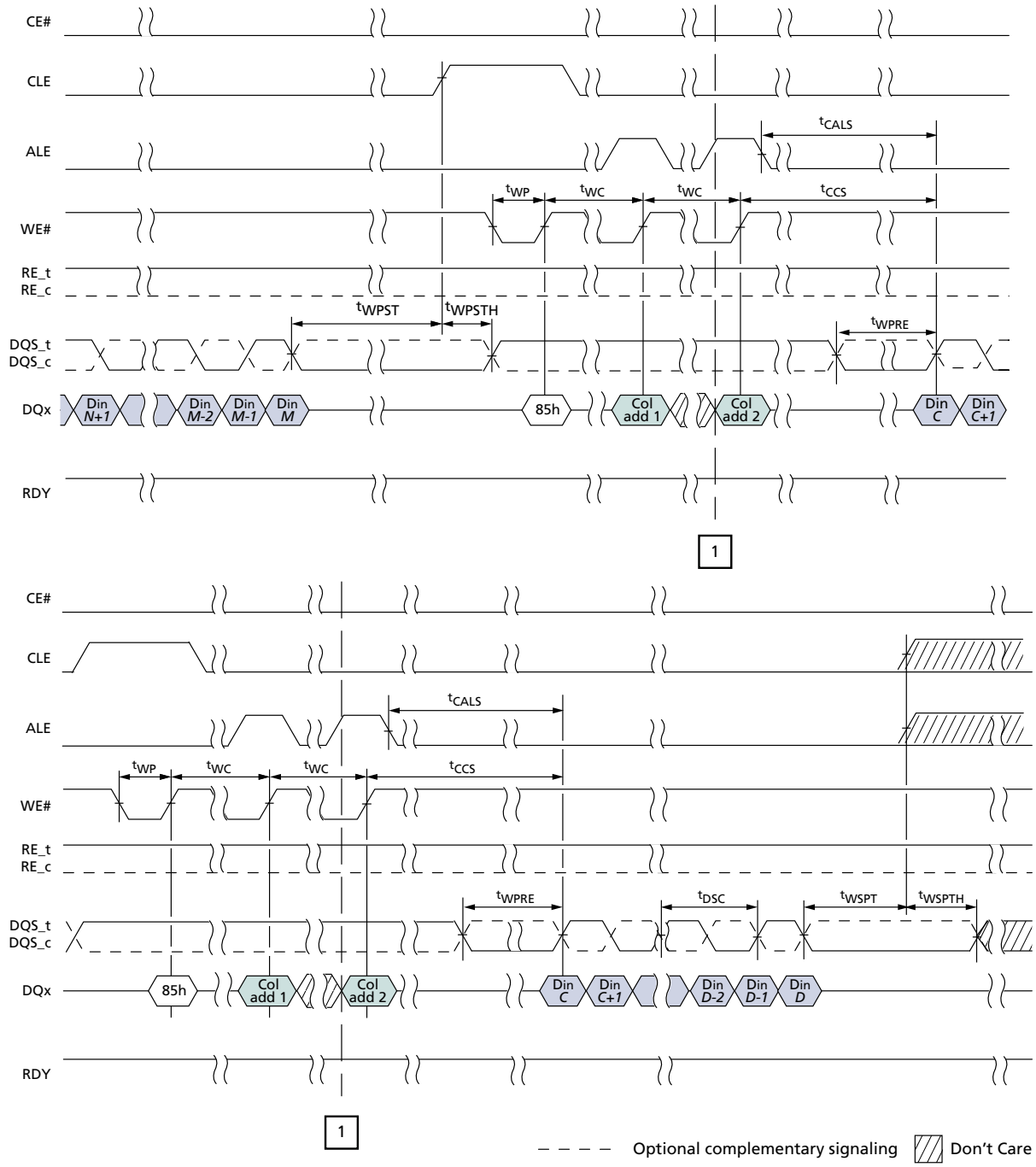
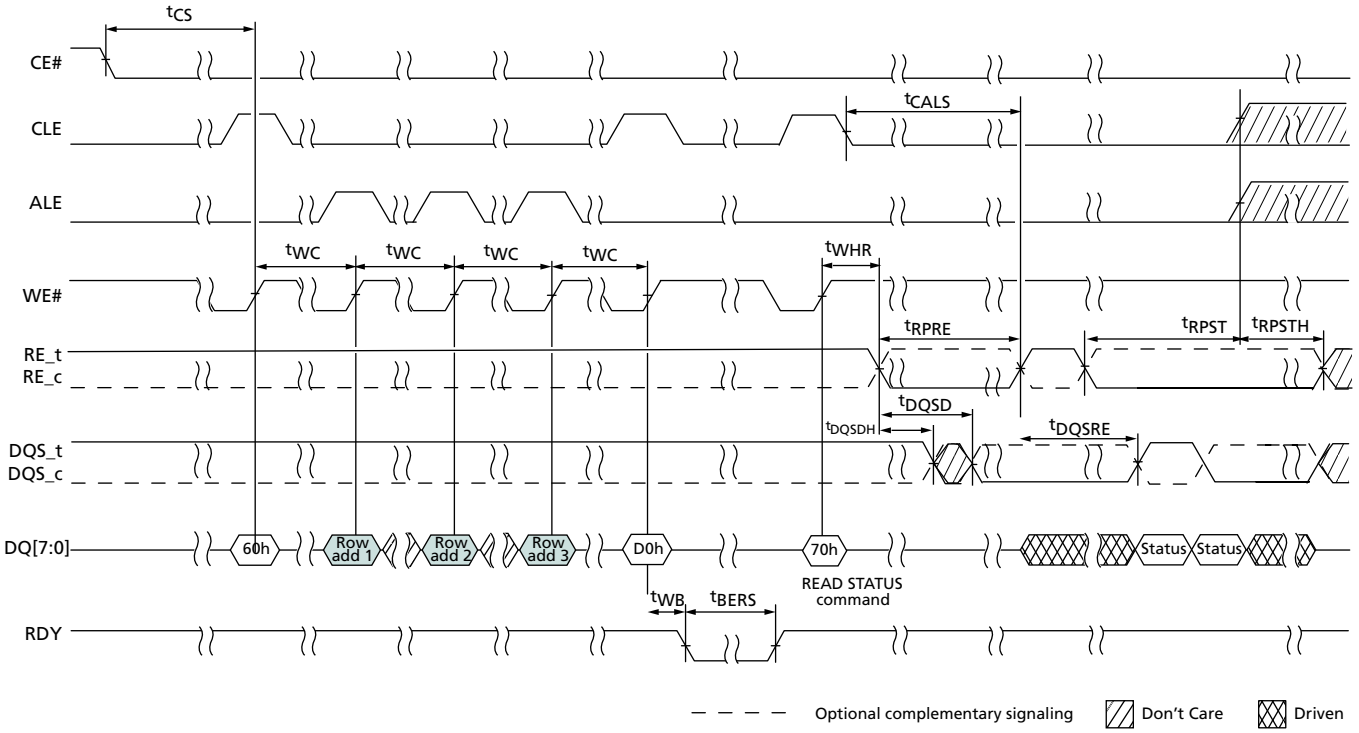
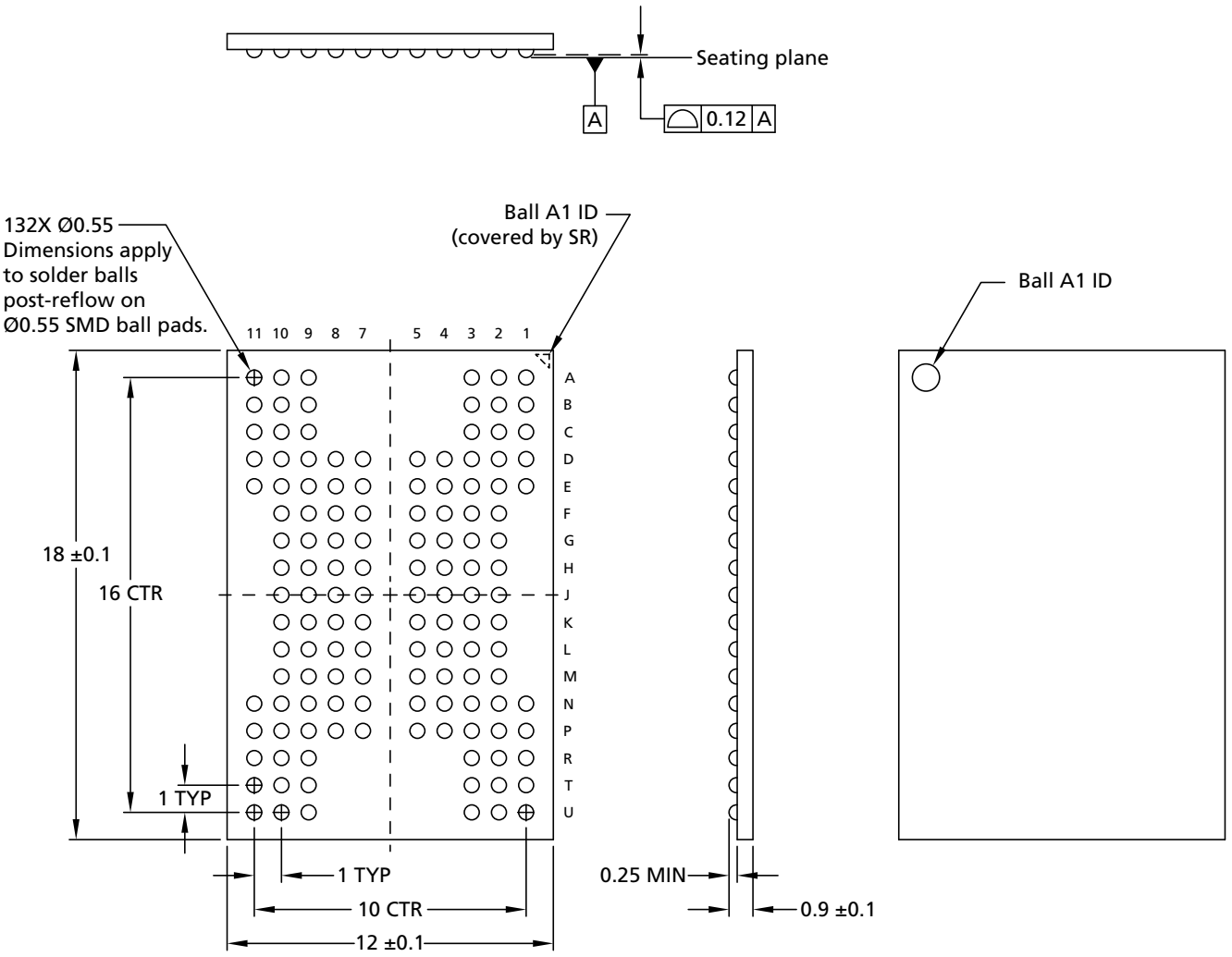


Figure 138: ERASE BLOCK



Package Dimensions

Figure 139: 132-Ball VBGA – 12mm x 18mm (J4 Package Code)



Notes: 1. All dimensions in mm.
2. Solder ball material: SAC405 (95.5% Sn, 4% Ag, 0.5% Cu).

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Revision History

Rev. A 04/2017

- SpecTek Initial Release.